LARGE AREA CRISTALLINE SILICON LPE THIN FILM SOLAR CELLS

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ABSTRACT: Large area crystalline silicon solar cells on thin epitaxial layers are investigated. The thin epilayers are grown by Liquid Phase Epitaxy (LPE) on cast multicrystalline silicon substrates. The wafer substrates are made from low cost metallurgical silicon feedstock. The electrochemical texturisation is employed for light trapping.
Keywords: Metallurgical – 1, Si Feedstock - 2, Thin Film - 3, LPE – 4, Texturisation – 5

1. INTRODUCTION

The availability of purified silicon for PV use and its cost will be main barriers for the development of PV market in the years to come. About 50% of crystalline Si-module cost are from the substrate cost. The substrate cost almost equally comes from silicon feedstock, crystallisation, and wafering costs. Using low cost upgraded metallurgical silicon for the high cost electronic grade silicon (EG-Si) can largely reduce the cost of silicon. The metallurgical silicon will be referred as photovoltaic graded silicon (PVG/Si).

In conventional silicon solar cell, the substrate is active absorber, whereas, in thin film silicon solar cell, the absorber is thin silicon layer epitaxially grown on the substrate. In thin film silicon solar cell, the low cost of substrate may offset the extra cost of the epitaxial growth of thin absorber layer. However, the advantage of thin film Si solar cell technology rely on the availability of PVG-Si which requires lower energy consumption and low capital investment production plant.

2. SILICON FEEDSTOCK DEVELOPMENT

The production of PVG-Si feedstock includes melting refining, of metallurgical grade silicon (MG-Si) supplied from an industrial production furnace. The refined MG-Si is then alloyed with Ca before casting. The solidified alloy is crushed into about 30-mm sizes. The lumpy Si-alloy then is leached with special leach liquor. The pure Si crystals are separated from the leach liquor and classified before packing. The product is granular silicon with main fraction in the range between 0.1 – 2.0 mm. Figure 1 shows schematic process steps for the manufacture of the PVG-Si feedstock.

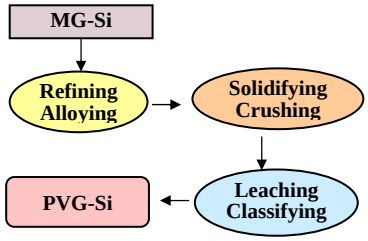

Fig 1. Process steps in the production of PVG-Si feedstock.

3. SUBSTRATE CRYSTAL GROWTH & WAFERING

The PVG-Si powder with a size range of 0.1 to 2.0 mm is melted and directional solidified in the Crystalox DS250 furnace (Figure 2). The material is put into a cylindrical crucible, which beforehand have been coated with three layers of Si_3N_4 and heated to 700 ºC for 10 hours. The crucible has an inner diameter of about 25-cm and a height of 22 cm and about 10 kg of silicon can be melted in each batch.

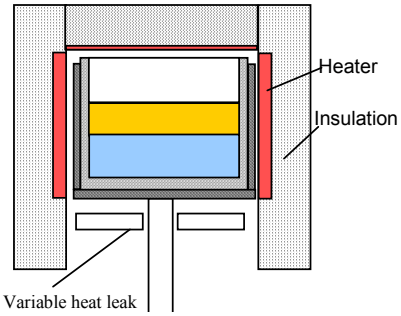

Fig 2. Schematic view of the central part of the Crystalox DS250 furnace.

All the equipment (furnace, crucible) and preparation (coating, melting) take place in a clean room environment satisfying a 10000 part/ft requirement. The crystal growth is controlled by temperature, crucible translation and a variable heat leak system in the bottom of the furnace. A typical cycle time for the heating, melting, solidification and cooling of the silicon material is 40 hours.

From the ingot either one or two 10 x 10 cm^2 blocks are squared out with further cutting off the bottom and top parts. Wafering is performed at an industrial location with a wire saw equipment to wafer thickness in the range of 300-350 µm. Average resistivity of the wafers are about 15 mΩcm corresponding to a dopant density of about $5 \cdot 10^{18}$ cm^{-3}.

4. LPE LAYER GROWTH

In previous activities [1, 2] it was shown the possibility of producing crystalline thin layer solar cells,

based on the low cost upgraded metallurgical silicon substrate, by using Liquid Phase Epitaxy (LPE). An about η = 10 % efficiency without surface texturisation (calculated potential: η > 14 %) was achieved. With former equipment it was possible to grow either three 5 x 2.5 cm^2 LPE-layers in one batch or one 10 x 10 cm^2 layer on the surface of the solvent. In view of later industrial applicability of this technique a new LPE construction was designed and built, which allows a wafer size of 10 x 10 cm^2 and an explicit larger number of wafers. While first deposition experiments on 5 x 5 cm^2 wafers were realized a special carrier for 10 x 10 cm^2 was developed. Today it is possible to work with up to 54, 10 x 10 cm^2 wafers in one batch.

To grow these layers the process steps shown in Fig 3 (from left to right) is employed.

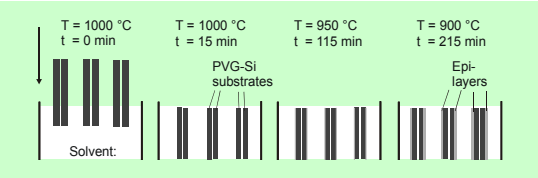

Fig 3. Principle of the Si-LPE growth for epi-layers on PVG-Si based wafers are loaded back to back for one-sided growth. In bifacial solar cells, both sides could be coated.

The indium solvent was saturated with Si at 900°C and afterwards heated up to 1000°C. Then wafers were placed into the melt, such that the melt was saturated again from Si of the substrate resulting in thinning of the wafer of about 30µm for each side. By cooling down the melt the LPE layer was grown. The highly doped substrate enables easy formation of the back contact, whereas the LPE layer acts as an active solar cell absorber. Residual impurities are expected to remain in the solvent because of the different solubility in epitaxial growing Si and the melt. A small amount of Ga was added to the In solvent to get a suitable p-dopant concentration in the active layer. To grow an industry relevant throughput of epi-layers on 10 x 10 cm^2 wafers by the new LPE reactor, still development work is needed. The most important task is how to place the wafers in the determined dimensions of the crucible and related to the carrier design as shown in Fig 4.

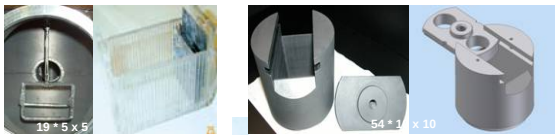

Fig 4. Carrier development for 5 x 5 cm^2 (quartz) and 10 x 10 cm^2 (graphite).

For first tests a hand made carrier from quartz glass was built for 19 wafers of 5 x 5 cm^2. Then the required specifications for an ideal carrier was formulated. The design was give the possibility of slow rotation of the carrier within the melt, to achieve temperature homogeneity during growth. An important question is to find an adequate material. Graphite works better than quartz, but there are still problems, e.g. oxidation of the silicon surfaces, which can be minimized by keeping the carrier in inert gas. A graphite carrier system is now in use, where partly surface treated by pyrolysis, which solves e.g. the oxidation problem. The new system is improved in detail, e.g. two clamp holes are needed as a melt reservoir because of the temperature depending density of the melt.

Several LPE experiments with a well defined melt were carried out on 10 x 10 cm^2 substrates. Main problem are the pinholes in the grown Si LPE layer on large area Si substrate. In Fig 5 two microscopic surface pictures of LPE layers are shown:

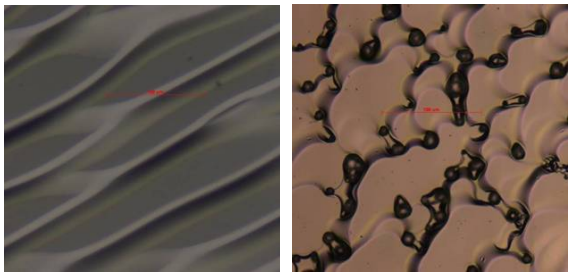

Fig 5. Left: Close LPE layer reached with former equipment for 5 x 2.5 cm^2 wafers. Right: typical LPE-layer on 10 x 10 cm^2 wafer with pinholes of Ø ≈ 25µm. (edge of pictures ~270-µm)

Improvements of growth parameters with a slight over-saturation lead to some mm^2 of pinhole free LPE layers on 10 x 10 cm^2 Si substrates (Fig 6).

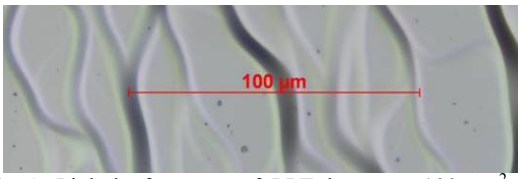

Fig 6. Pinhole free part of LPE layer on 100 cm^2 Si substrate.

Further improvements of the LPE procedure lead to closed areas of some cm^2 on 100 cm^2 Si substrates and recently two 100 cm^2 probes with about 90 % "closed" LPE layer have been realized. Fig 7 shows a scan of one of them. Its surface looks as smooth as glass, which is typically for pinhole-free LPE-layers:

Fig 7. A 10 x10 cm2 mc wafer with "closed" LPE layer.

A microscopic surface picture of Fig 8 shows that there are only very small craters in the grown LPE surface of about Ø ≈ 5µm.

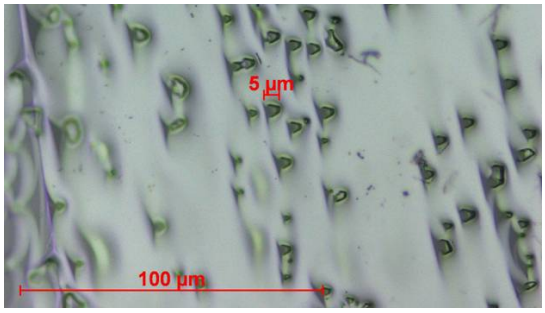

Fig 8. Microscope picture of LPE grown surface.

Microscopic cross section pictures shows that these craters have a depth of about 5µm. The thickness of the epi-layer was measured after selective etching of the cross section and resulted in about 20 µm layer thickness as compared to the theoretically calculated epi-layer thickness of 30 µm. The pinhole free LPE layers covering almost the whole 100 cm^2 wafer area where reached by 4 serial meltback and regrowth steps [3]. This successive growth technique may cause a sequence of four epi-layers with the pinholes be forced to grow out of existence.

Although these two successfully grown layers were reached on commercial mc-Si wafers it would be possible to grow such layers on PVG-Si wafers as well, because of similarity in growing on commercial mc-Si with PVG-Si based wafers.

5. ELECTROCHEMICAL TEXTURISATION

The decrease of the silicon reflectivity is a major task to perform, to obtain high efficiency solar cells. An efficient texturisation will become more important as future Si solar cells will be thinner and will require efficient light trapping methods to maintain good absorption of the infrared light. The electrochemical oxidation of p-type Si in mixtures of hydrofluoric acid (HF) with specific organic solvents leads to the formation of a macroporous layer [4, 5], which is very efficient in lowering the reflectivity. The technique texturizes all the grains with microstructures in the micrometer range and overall the morphology is somewhat similar to that obtained with the dry reaction ion etching process. It has the advantage over chemical etching that the reaction can be controlled by the applied current density and that the results are easily reproduced. The thickness of the dissolved layer depends only on the applied current and the treatment time. We found that for an efficient texturisation, a silicon layer less than 3-5 µm thick has to be removed. The electrochemical macroporous texturization appears then to be a very suitable technique to texturize the surface of the 30 µm thick multicrystalline layer epitaxied on the Up grade PVG-Si substrate (Fig 9). The electrochemical texturisation is very sensitive to the silicon doping level in the 2-0.02 Ω-cm range. First, macropores does not form on silicon with a 0.02 Ω-cm resistivity, while in the 2-0.2 Ω. cm resistivity range the average effective reflectivity of a macroporous texturized multicrystalline silicon surface varies from 16 to 9%, respectively (Fig 10). Results on 5x5 cm^2 p-type silicon epi-layer grown on mc-EG Si substrate show that 10.3 % effective reflectivity (AM1.5, 400-1000 nm) can be achieved after macroporous texturization (Fig 11) against 27 % for the untreated surface.

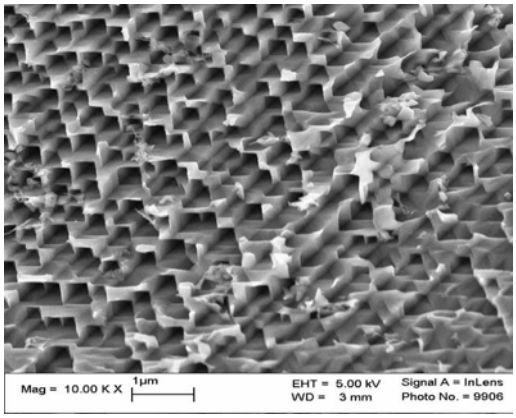

Fig 9. SEM image (plan view) of the electrochemically macroporous texturized surface of a LPE layer in a region showing two grains with different (100) and (111) crystalline orientations

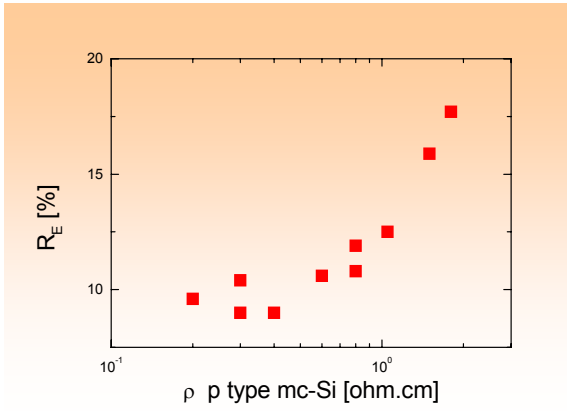

Fig 10. Variation of the effective reflectivity of macroporous texturized multicrystalline p-type silicon as a function of the silicon resistivity.

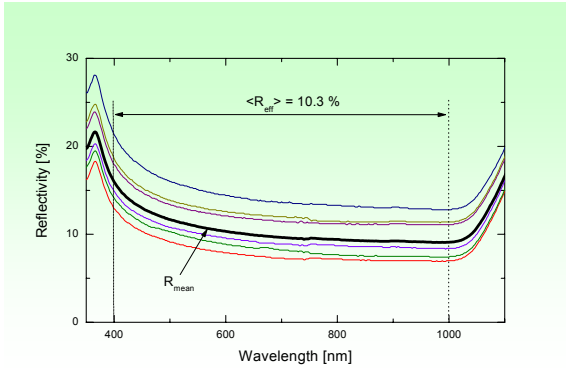

Fig 11. Reflectivity spectra measured on 10 spots of a macroporous texturized LPE layer grown on EG mc-Si substrate with ρ=0.3 Ωcm. Average effective R=10.3%.

Even the long passivation time of 24h is not sufficient to detect D throughout the whole bulk. A symmetrical shape of the profile is observed as with the MIRHP technique D diffuses from both surfaces (emitter and Al-covered backside) into the sample. The slope of the profile and the low penetration depth again indicate a trapping mechanism during D-diffusion.

6. SOLAR CELL DEVELOPMENT

For solar cell optimisation doping profiles of LPE layers were investigated. Therefore after some mm^2 of close LPE layers on PVG-Si could be realised ECV (Electrochemical Capacitive Voltage) profiles were recorded.

PC1D simulations were used to determine the target epi-layer carrier concentration profile (Fig 12). The gradient profile over two orders of magnitude through the active layer causes a strong drift field and therefore enhances the effective diffusion length even when lifetimes of τ=0.5 µs are considered. With this parameters and the measured reflectivity of the epi-layer after electrochemical macroporous texturisation, efficiencies of 14% and higher should be feasible.

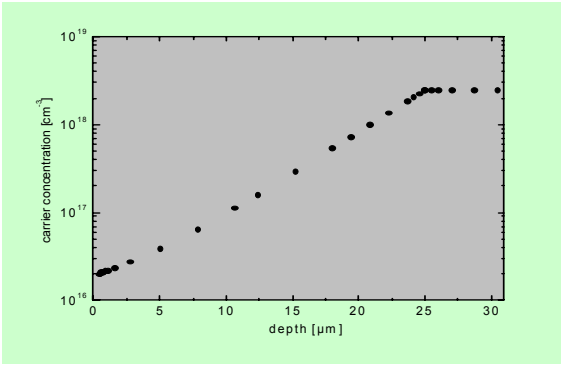

Fig 12. Target doping profile in LPE layer simulated by PC1D.

Fig 13 shows the experimental carrier concentration profile achieved so far after fine tuning of the LPE process parameters, such as growth rate and temperature range. The surface concentration of ~3 x 10^{16} cm^{-3} should enable effective emitter formation by phosphorous diffusion.

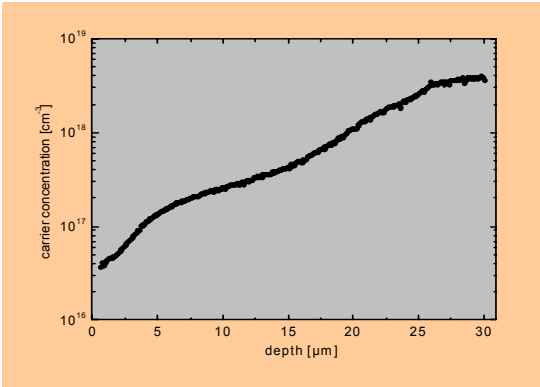

Fig 13. Doping profile of LPE layer deposited on upgraded metallurgical Si measured by ECV.

Test solar cells of $25cm^2$ size were processed by $POCl_3$ diffusion, SiN deposition, and screen printing and firing through. Unfortunately the cells were shunted through the pinholes present in some areas as described above (Fig 14).

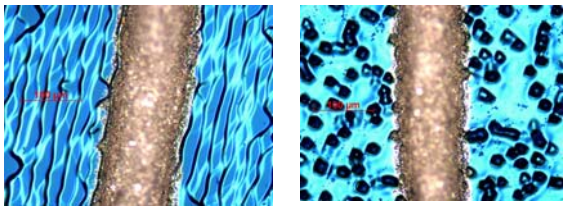

Fig 14. LPE solar cell showing areas with and without pinholes

If the recently grown epi-layers on large area without pinholes could be reproduced on suitable PVG-Si wafers, reasonable crystalline thin film solar cells should be feasible.

7. CONCLUSION

The availability of purified Si for PV power production at large scale and its cost will be main barrier for the future development of PV market. The low cost and abundant upgraded metallurgical PVG-Si appears to be a suitable feedstock for the production of wafer substrate for thin film silicon solar cells and modules. It is expected that solar cell of target performances could be achieved with the overcoming of the pinhole problem.

8. ACKNOWLEDGEMENTS

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9. REFERENCES

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