# THE EUROPEAN PROJECT 20PLµS: 20 PERCENT EFFICIENCY ON LESS THAN 100 µM THICK INDUSTRIALLY FEASIBLE CRYSTALLINE-SI SOLAR CELLS

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ABSTRACT: The European project 20plµs is developing Si wafer solar cells with efficiencies above 20% on wafers less than 100 µm thick. Three principal solar cell process routes are investigated. The three approaches are distinguished by the doping type and maximum process temperature: p-type monocrystalline Cz-Si and multi-crystalline Si solar cells subjected to high temperature processes are called pht, and n-type Cz-Si cells fabricated with low and high temperature processes are called nlt and nht, respectively. Already at the project's midterm, a particular pht solar cell process was transferred to pilot line production. Key issues such as wafering, surface passivation, light trapping, metallisation and life cycle analysis were tackled to determine which process should be transferred. To date, by integrating the processes investigated within the project into full solar cells, efficiencies up to 18.7% (pht), 19.0% (nht) and 20.8% (nlt, 4 $cm^2$) have been achieved on 100 µm thick large area Si wafers.
Keywords: thin Si wafer, light trapping, high efficiency

## 1 INTRODUCTION

The reduction of cost per Watt-peak (Wp) is most efficiently achieved for silicon solar cells by reducing silicon material cost using thin wafers *and* enhancing the efficiency to above 20%. However, today´s standard industrial cell structures are not suited to reaching this goal. Additionally, the mechanical yield of the solar cell and module production has to be high to reach cost effectiveness, which is difficult for thin wafers. Therefore the approach of the 20plµs project ***"20 percent efficiency on less than 100 µm thick industrially feasible c-Si solar cells"*** is to achieve efficiencies exceeding 20% by applying new solar cell structures and processes adapted both to industrialization and to the special needs of wafers which are less than 100 µm thick.

Already at midterm of the project, a high-efficiency process selected from three solar cell fabrication routes is determined to be transferred to a pilot production line of the industrial partner Q-Cells.

## 2 OBJECTIVES

The overall objective of this project, which started in October 2010 and has a duration of 36 months, is the development of a 20%-efficient silicon solar cell with a thickness below 100 µm. The process will be transferred to a pilot line at Q-Cells, aiming at a yield comparable to the standard production yield and a conversion efficiency of 19.5% on 100 µm thick solar cells with an area of 156 × 156 $mm^2$.

The silicon photovoltaics sector has seen acceleration in the transfer of results from laboratories to large-scale manufacturing, in particular, of processes that reduce wafer thickness and increase solar cell efficiency. This has been a very good strategy, as silicon accounts for about 35% of the module cost today [1].

The average silicon consumption has shrunk from about 11–12 g/Wp only a few years ago, to about 8 g/Wp today. Equivalently, the wafer thickness has been reduced from 330 µm to around 200 µm while more than doubling the cell surface area to the current 225 $cm^2$.

Of course, the average silicon consumption is an imperfect metric and does not reveal details such as best practices in industry, yields at different manufacturing sites, and differences in technologies, and may thus lead to large deviations in demand prediction even with a modest uncertainty of ±1 g/Wp [2]. Nevertheless, it is still a good indicator of a trend in industry and is one of the parameters used by the European PV Platform to monitor further progress of silicon-based photovoltaics in its roadmap for reaching full competition with conventional energy sources [3].

This project aims to enable a technological leap by halving the wafer thickness while keeping the efficiency. Preliminary considerations show that this thickness reduction corresponds to a silicon consumption drop to 5–6 g/Wp; that is, about 30% less overall consumption given the conservative assumption that wire diameter — and hence kerf loss — and wafering yield do not decrease significantly. If we add the effect of an efficiency increase as well, the specific consumption drops to the 3 g/Wp range, thereby implying the feedstock cost would drop to 0.15–0.20 €/Wp. As of today's solar grade Si spot market price of 20–25 €/kg [4], this reduction in

feedstock cost will allow for crystalline Si module production costs below 0.5 €/Wp.

2.1 Specific objectives

The 20plµs project deals with the full process flow, addressing in more detail topics which are particularly crucial for solar cells on thin Si wafers. These include wafering, surface passivation, light trapping, solar cell and module processing and handling of the thin wafers. The specific objectives follow.

The *wafering* of the Si ingots is performed by the established wire sawing process using advanced technologies. Handling is investigated from the ingot to the process-ready wafers. The *mechanical stability* of the wafers is optimized by applying different wet-chemical treatments. Breakage tests are carried out, assessing the impact of sawing and etching parameters on wafer strength. The target is to demonstrate a yield as high as that for standard wafering, but at lower thickness. The handling of thin and ultra-thin wafers is somewhat different. While 100 µm thick wafers can still be handled using adapted, standard techniques, wafers with thicknesses of around 50 µm might need a support structure and are preferably handled horizontally. A feasible handling system for each of the two thicknesses is defined and tested. A handling throughput of 1500 wafers/h is demonstrated.

When the wafers become thinner, *surface passivation* becomes crucial, because more and more minority charge carriers reach a surface and their recombination needs to be avoided. Therefore, we aim to develop the most suitable passivation layer with regard to the industrial feasibility of the deposition method and the passivation as well as antireflection-relevant properties.

Because of the indirect bandgap of Si, absorption of 900–1200 nm infrared light decreases with decreasing wafer thickness. Therefore, device structures incorporating the best optical approaches for minimizing the associated current loss are quantified and validated. *Advanced light trapping schemes* are subsequently implemented.

Solar cell processes are evaluated taking into account industrial feasibility, and thus the time to bring the process into production as well as the efficiency potential. The main objective here is to find the best compromise between light trapping, surface passivation, emitter design, metallization, bulk lifetime and handling resiliency. In particular, the *selective emitter* and *hetero-emitter* approach are investigated. Low-mechanical-impact metallization techniques like *metal jet printing* and *plating* are evaluated.

Based on the results of the first 18 months of the project, an industrial solar cell process is defined and transferred to the pilot production line.

2.2 Routes for solar cell development

There are three main routes for solar cell development pursued within this project for cells both 50 µm and less than 100 µm thick. The three approaches are distinguished by the doping type and maximum process temperature: p-type mono- and multicrystalline Cz-Si solar cells subjected to high temperature processes are called pht, and n-type CZ-Si cells fabricated with low and high temperature processes are called nlt and nht, respectively. Figure 1 gives an overview of possible solar cell concepts in accordance with the three main routes.

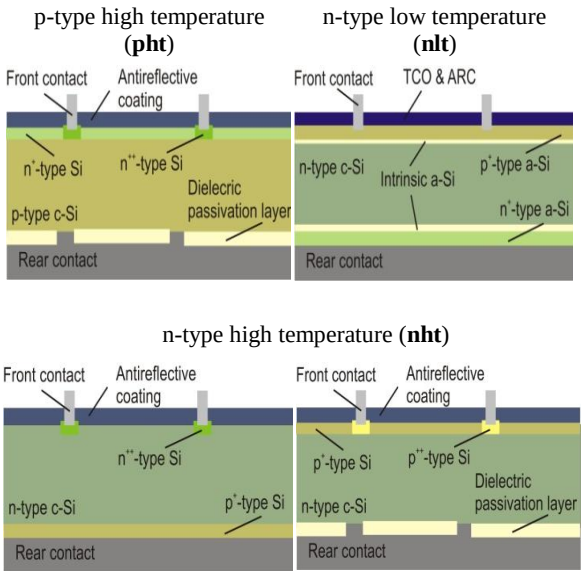


**Figure 1:** Solar cell concepts of the three main routes for which solar cell processes are developed within the 20plµs project: pht, nlt and nht.

3 RESULTS

3.1 Wafering from Si ingots

One of the major aims of this work is to evaluate adequate wire sawing process parameters. Therefore, several parameter studies were conducted with a focus on the wire tension, the wire, and the size of silicon carbide (SiC) particles as well as the ratio of wire and particle diameter.

The total thickness variation (TTV), the roughness and the average induced crack lengths of the sawn wafers were measured. With a higher wire tension the vibrations of the wire were reduced. The wire-to-SiC diameter ratio has to be within a certain range to reduce surface roughness and limit the length of induced cracks due to the differences in the material removal process in comparison to the standard industrial process.

In figure 2 a photograph of a slurry-sawn wafer (left) and a diamond-wire-sawn wafer (right) is shown. The slurry-sawn wafer has a matt finished surface, whereas the diamond-sawn wafer has a shinier surface. The different material removal mechanisms are responsible for this effect. The slurry-based process relies on the brittleness of the material, as SiC particles indent into the silicon surface and induce cracks which are responsible for the material removal. The diamond-wire-based process is dominated by a ductile material removal process, in which fixed abrasive particles plastically deform the silicon surface and thereby remove the material. A layer of amorphous silicon can be formed on the wafer surface during this process. It is expected that this difference in surface morphology may have a significant influence on the cleaning processes after wire sawing and the texturing step during solar cell processing.

A second important difference of the surface quality is the homogeneity and roughness. The Si-wafers sawn with diamond wire show a regular pattern of small parallel saw marks in the direction of the wire. This can be seen in figure 2 (right) as dark stripes parallel to the

horizontal wafer edges. The reason for this is the alternating direction of the wire movement after a defined length of used wire during the cutting process. At defined time intervals, the wire speed is diminished and the direction of wire movement is reversed. This bidirectional cutting process (known as "pilgrim mode") is applied in order to optimize the utilization of the costly diamond wire. In contrast, the wire movement for the SiC slurry process is unidirectional throughout the whole process resulting in more homogenous surface properties.

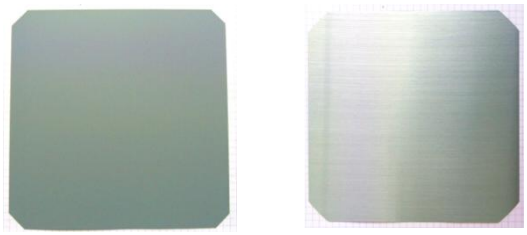

**Figure 2:** Photograph of 156×156 mm² pseudo-square monocrystalline silicon wafers sawn with a slurry process (left) and a diamond wire process (right).

3.2 Handling

As a first step toward the evaluation and adaption of a suitable handler for wafers ≤ 100 µm thick, a demonstration unit was developed. The handler's functions shallinclude wafer separation, belt placement and transfer between carriers. Bernoulli-based handlers were identified as the most suitable for thin wafers.

3.3 $j_{0e}$ of high-temperature emitters

The three high-temperature emitters were B-diffused, P-diffused and Al-alloyed from a screen-printed paste. B- as well as P-diffused emitters both exhibited a sheet resistance of 100 Ohm/sq. The P-diffused emitter was etched back, which led to a saturation current density $j_{0e}$ of ~100 fA/cm$^2$ before and ~40 fA/cm$^2$ after firing for 5 s at 900 °C in a conveyor belt furnace.

The B-diffused emitter is passivated by an alumimum oxide ($Al_2O_3$) layer deposited by plasma-enhanced chemical vapor deposition (PECVD) or atomic layer deposition (ALD). The passivation quality is similar to that of the P-emitter, and there is a remarkably linear behavior over an injection range between 1 and $4.5 \times 10^{16}$ cm$^{-3}$ [5]. The fit leads to a $j_{0e}$ value of (36 ± 1) fA/cm$^2$. For the Al-doped $p^+$ emitter featuring an additional $Al_2O_3$ surface passivation, we have achieved $j_{0e}$ values of 55 fA/cm$^2$ [6].

The Al-doped emitter was almost 6 µm deep with a concentration that increases from $1 \times 10^{19}$ cm$^{-3}$ at a depth of 0.5 µm to $2 \times 10^{19}$ cm$^{-3}$ at 5 µm. The Al-doped emitter, which is epitaxially grown during firing of screen-printed Al paste, was passivated by $Al_2O_3$, and the other side of the wafer is passivated by a P-diffused layer. For this sample, an emitter saturation current density of 150 fA/cm$^2$ was estimated.

3.4 Surface passivation

For p- and n-type Si substrates (1 Ωcm) passivated with an $Al_2O_3$ layer deposited by ALD, the measured lifetimes at an excess carrier density of $10^{15}$ cm$^{-3}$ indicate maximum surface recombination velocities of below 5 cm/s and 3 cm/s, respectively. For both p- and n-type Si surfaces, excellent surface recombination velocities below 6 cm/s *after the firing process* were achieved. This result was achieved with a passivation layer consisting of a stack of an ALD $Al_2O_3$ layer covered by a PECVD silicon nitride ($SiN_x$) layer. The firing process took place in a commercially available firing furnace at standard contact firing conditions.

The effective lifetime at $10^{15}$ cm$^{-3}$ is not the only criteria for high passivation quality; the lifetime should also be nearly constant over a large injection range. All partners except EPFL used an ALD-$Al_2O_3$-based passivation layer in a "lifetime competition" on p-type Si wafers. EPFL applied an amorphous-silicon-based passivation. The samples prepared by ISE showed the highest lifetime over a small injection range centered around $10^{15}$ cm$^{-3}$, while the samples from EPFL peaked at a higher injection level of about $2 \times 10^{15}$ cm$^{-3}$. From this data, we determined which passivation layer would allow for the highest efficiency. The injection-dependent lifetime data can be interpreted as an implied current-voltage characteristic [7]. Assuming a short-circuit current density ($j_{SC}$) of 40 mA/cm, the "implied performance" of solar cells with the passivation layers from the competition are presented in table I. The Si wafer passivated with amorphous silicon (a-Si:H) has the highest implied open-circuit voltage ($V_{OC}$), but the lowest fill factor (*FF*) due to low lifetimes at low injection, indicating the importance of the lifetime at all injection levels.

**Table I:** Implied $V_{OC}$, *FF* and efficiency ($\eta$), assuming $j_{SC}$ = 40 mA/cm$^2$.

| Partner – sample | $V_{OC,\ impl.}$ (mV) | $FF_{impl.}$ (%) | $\eta_{impl.}$ (%) |
|---|---|---|---|
| ISE | 726 | 81.9 | 23.78 |
| UKON | 724 | 81.7 | 23.66 |
| PVT | 719 | 82.1 | 23.61 |
| EPFL | 727 | 80.5 | 23.41 |

For a-Si:H based layers it was demonstrated that the *silane depletion* is a very important parameter for the passivation quality [8]. By depositing intrinsic (i) and doped (n or p) a-Si on 100 µm thick n-type FZ-Si wafers, implied $V_{OC}$ values of up to 752 mV have been demonstrated (741 mV using 160 µm thick n-type Cz-Si wafers).

The implementation of a *hydrogen plasma treatment* in the deposition process of a-Si:H leads to a "layer by layer deposition" [9]. This process allows one to increase the hydrogen content and the disorder in the film, keeping the deposition process at the very edge of the transition between a-Si:H and microcrystalline silicon (µc-Si:H). The implementation of this new process results in an extraordinary increase of the passivation quality of the a-Si:H layers.

3.5 Light management

Simulations were performed of nanostructured rear reflectors consisting of a grating intended to obliquely scatter light, thereby reducing the light that escapes from the wafer surface. The optimum grating gave a current density gain of 1.8 mA/cm$^2$ compared to a flat back side.

A honeycomb texture fabricated by nanoimprint lithography (NIL), and plasma etching yields nearly the same front reflectance as inverted pyramids, but can be performed on multicrystalline Si wafers [10]. A sun-spectrum-weighted reflectance of only 14.6% (no anti-

reflection coating) was demonstrated, which is significantly lower than that achieved with an isotropic texture (figure 3) [11].

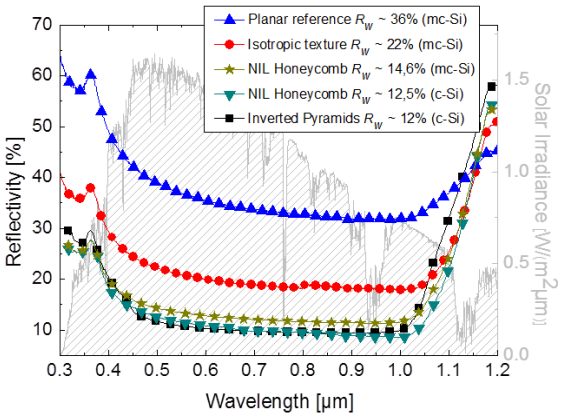


**Figure 3:** Reflection measurements of various textured wafers without anti-reflection coatings. In the background, the solar AM1.5g spectrum is shown, with which the reflection measurements are weighted [11].

For nlt cells, we performed a complete experimental analysis of all $j_{SC}$ losses in a high-efficiency (>20%) cell 96 µm thick. Active-area and aperture-area $j_{SC}$-values were measured and compared to reveal that 6% of light is reflected from the front silver grid, corresponding to a $j_{SC}$ loss of 2.2 mA/cm$^2$. EQE and reflection measurements showed that 1.1 mA/cm$^2$ is lost because of reflection from the front wafer surface, 1.5 mA/cm$^2$ remains to be gained by eliminating parasitic absorption in the front a-Si:H layers, 1.1 mA/cm$^2$ is lost because of parasitic absorption in the transparent conductive oxide (TCO) and rear metal reflector, and 0.6 mA/cm$^2$ can be gained by improving light trapping. This analysis provides a clear path to further improvement of $j_{SC}$ in thin nlt cells.

3.6 Metallisation

Electroless Cu plating of "Laser-Grooved Buried-Grid (front) – Laser-fired contacts (rear)" solar cells with a phosphorous emitter [12] was optimised such that a gridline resistance of < 0.3 Ω/cm, a finger width of < 50 µm and a contact resistance below 2 mΩcm$^2$ were achieved simultaneously.

A two-step Ni plating process on highly B-doped flat Cz-Si surfaces also resulted in a contact resistance below 2 mΩcm$^2$, and after copper plating, the 47 µm wide fingers had a line resistance of 0.45 Ω/cm [13].

For contacting emitters of nlt cells, screen- as well as stencil-printing techniques were applied, which yielded fingers that met the width and line resistance mentioned above.

3.7 Solar cells from the pht route

100 µm thick pht solar cells were fabricated with a screen-printing-based process with a selective emitter on the front and a full area Al back surface field at the rear. The front emitter was selectively etched back and then passivated by a thermal oxide/$SiN_x$ stack. After applying a regeneration process that recovers the bulk lifetime and the electrical parameters of the solar cells [14], the best cell showed an efficiency of 18.7% with a $V_{OC}$ of 645 mV, a $j_{SC}$ of 36.6 mA/cm$^2$ and a *FF* of 79.3% on a cell area of 151.5 cm$^2$.

3.8 Solar cells from the nht route

The "PhosTop" cell concept [15], in which the processing sequence for p-type solar cells is applied to n-type Si wafers, is a promising candidate for simple and low-cost fabrication of n-type Si solar cells. This approach produces a solar cell with a P front surface field and screen-printed Al-alloyed rear emitter. An independently confirmed efficiency of 19.4% was demonstrated on 180 µm thick 6" Cz-Si wafers [16]. For solar cells less than 100 µm thick, efficiencies of up to 19.0% were achieved by applying a similar process [17]. The best cell had a $V_{OC}$ of 651 mV, a $j_{SC}$ of 36.6 mA/cm$^2$ and a *FF* of 79.8% on a cell area of 148 cm$^2$.

3.9 Solar cells from the nlt route

n-type FZ-Si wafers were thinned to 96 µm (determined by mass) using a long saw-damage removal step before alkaline texturing. Intrinsic a-Si:H layers were deposited on both sides of the Si wafers using PECVD in a reactor operated at very high frequency (VHF, 40.68 MHz) [8,9]. These layers have been optimized on thick wafers to yield minority carrier effective lifetimes as large as 11 ms. p- and n-type a-Si:H layers were deposited on the front and back of the cell, respectively, to form the emitter and back surface field. The p-layer thickness was kept below 5 nm to minimize blue and UV parasitic absorption [18], while the n-layers were somewhat thicker. Hydrogenated indium oxide / indium tin oxide (IO:H/ITO) bilayers, which are high-mobility, low-contact-resistance TCO layers, were sputtered on both sides of the wafers. The cells were finished with a sputtered Ag reflector and a screen-printed Ag front electrode grid. All processes are industrially compatible.

The current-voltage (I-V) characteristic of the best 4 cm$^2$ nlt solar cell on a 96 µm thick wafer is shown in figure 4. The $V_{OC}$, *FF*, and $j_{SC}$ are given in figure 4 and reach 735 mV, 77.3%, and 36.7 mA/cm$^2$. The aperture-area efficiency is 20.84%, while the active-area efficiency exceeds 22%.

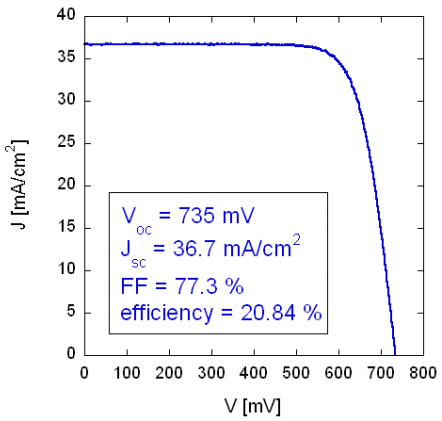


**Figure 4:** I-V curve of the best 4 cm$^2$ nlt cell on a 96 µm thick wafer. The electrical parameters of the cell are given.

3.10 Assessment

The present study is focussed on the industrial feasibility of the solar cells proposed within this project, that is *pht*, *nht* and *nlt* routes. The study takes into account scalability to a pilot line environment, life cycle

analysis (stage one) and cost estimation (rough) of the three processes.

In terms of scale-up, critical aspects of the three routes were explored for transferring the most suitable process into pilot production at Q-Cells facility. The pht route is the most feasible process to scale up, as it requires a lower number of new process equipment to be installed at Q-Cells production site within the development timeline of the project.

The life cycle analysis is based on a model which takes into account ingoing and outgoing flows. More precisely, the system *includes*: main process (solar cell production); energy supply (mainly electricity and power supply, thermal energy); raw materials; treatment of emissions and wastes. Instead, silicon production as well as wafering, cells assembling into modules (or packing of cells), PV-installation and transportation are excluded.

Environmental aspects are evaluated with GaBi software [19]. Impacts were assessed on the basis of the EDIP method [20-22].

The pht route turns out to be the process with the best environmental performances.

Cost analysis takes into account fixed and variable costs. Fixed costs are due to equipment, infrastructure and labour expenses. Depreciation of equipment, facility and building were also included in the cost calculation. Variable costs included expenses for materials, consumables, utilities and wastes.

In addition, mechanical and optical/electrical yield losses were estimated in the calculation. Especially, mechanical yield loss turns out to play a relevant role in terms of costs as it is due to wafers breakage rather than a lower performance of the cells.

The pht route turns out to be the process with the lowest operating costs.

## 4 CONCLUSION

The 20plµs project not only deals with straight-forward developments that are directly based on industrial standards, but also with new structures to determine which is the perfect structure for the next generation of industrial high-efficiency solar cells. The results mentioned above, in addition to those not presented here, provided the basis for further developments and the decision to transfer the pht route to the pilot production line.

The individual process steps allowing a solar cell efficiency of 20% on monocrystalline CZ-Si have been demonstrated to be ready for implementation in a full solar cell process. The first solar cell results demonstrate the excellent efficiency potential unique to 100 µm thick Si wafers.

Currently, the first solar cell steps are about to be transferred to the pilot production line.

## 5 ACKNOWLEDGEMENTS

The collaborative project “20 percent efficiency on less than 100 µm thick industrially feasible c-Si solar cells” (20plµs) is funded by the European Commission under FP7 with the contract number 256695.

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