THE DEVELOPMENT OF ETCH-BACK PROCESSES FOR INDUSTRIAL SILICON SOLAR CELLS

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ABSTRACT: The exactly controlled wet-chemical etch-back of diffusion profiles can shift the efficiency limit of the widely used screen printing process to higher values. In conjunction with an inkjet or screen printing masking step, the cost effective production of selective emitter solar cells is possible. We present the development of our etch-back process using Cz-Si and mc-Si wafers. Emitter saturation current densities of etch-back emitters are lower compared to directly $POCl_3$-diffused samples with the same sheet resistance. Negative effects of the etch-back process on reflection properties are negligible if less than 90 nm are removed from the surface. Grain boundaries of mc-Si wafers may be etched faster than the rest of the wafer. A screen printed 5 inch Cz-Si selective emitter solar cell with full area Al BSF reached an efficiency of 19.0%. The same process was applied to n-type Cz-Si wafers with a selective front surface field (FSF) and a full area screen printed Al emitter. An efficiency of 18.5% on 6 inch n-type Cz solar cells could be reached in a first test. This emphasizes the highly effective FSF and makes the process attractive for possible industrial production, since no boron-oxygen degradation occurs in n-type silicon.
Keywords: Selective emitter, n-type, c-Si

1 INTRODUCTION

In the last few years there was no significant change in the standard process scheme of industrially produced screen printed silicon solar cells. New technologies to improve the front side of the solar cell are now introduced into industry. Beside the improvement of the baseline process by optimizing the system of emitter, SiN_X:H surface passivation and new pastes to contact higher sheet resistances, there are two major development paths: one of them is the 'seed & plate'-technology [1]. A silver ink which is able to contact high sheet resistance emitters is deposited by aerosol or inkjet printing and fired to form the contact. An additional plating step is needed to improve the line resistance of the metallization. The other technology is the introduction of a selective emitter design. The highly doped area underneath the finger is easy to contact with conventional silver pastes and the lowly doped area between the metallization grid minimizes the recombination on the front side. Several technologies are on the market to form the selective emitter structure, some are compatible with plating technologies to form the contact [2-6]. A status of selective emitter technologies is given in [7]. This paper gives an overview of the development of an etch-back selective emitter structure developed at the University of Konstanz. This structure can also be used as a selective front surface field.

Former experiments [8], where process schemes for selective emitter structures were investigated, revealed that especially a well controlled etch-back of $POCl_3$ emitters led to very low saturation current densities. The etch-back process can be used to improve the doping profile and lower the phosphorous surface concentration. Measurements of emitter saturation current densities were carried out on symmetrical samples with different initial doping profiles to determine the best suited doping profile. The reflection properties of etch-back samples are also investigated and possible j_{SC} losses have been addressed. Grain boundaries of mc-Si wafers have been studied with SEM (Scanning Electron Microscopy) before and after an etch-back to detect a possible preferential etch. Selective emitter solar cells were processed and the efficiency evolution is being presented. The selective etch-back process is also suited to form a selective front surface field by using the same process beginning with n-type silicon wafers [9]. The emitter is in this case formed by alloying screen printed aluminum on the rear. This cell concept was introduced by Meier et al. as "PhosTop" [13]. To obtain high efficiencies, both a high minority carrier lifetime of the bulk material and a low front surface recombination velocity are needed. 6 inch n-type Cz-Si solar cells with selective FSF and with a uniform FSF are processed and compared.

2 EXPERIMENTAL

2.1 Etch-back emitter

A diffused phosphorous doped emitter as used in industry has the typical kink-tail profile. Phosphorous surface concentration and depth can be varied by changing diffusion parameters like temperature, dwell times and gas flows when using a $POCl_3$-diffusion. Due to the high phosphorous surface concentration, Auger recombination is the dominating loss mechanism in the emitter. A certain emitter depth is wanted to obtain the lateral conductivity needed in a solar cell design. In Fig. 1 a well optimized 52 Ohm/sq emitter profile used in a screen printed solar cell process can be seen. Phosphorous surface concentration is about $4x10^{20}$ cm^{-3} measured by SIMS. A highly doped 17 Ohm/sq Emitter can be obtained by rising the diffusion temperature. By introducing an etch-back step, the phosphorous concentration on the surface [$P_{Surface}$] can be lowered.

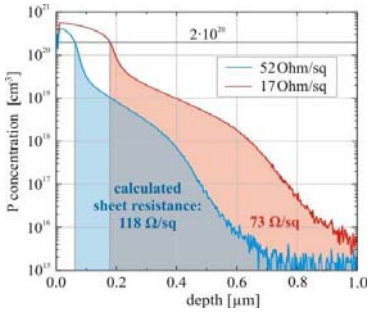

Figure 1 SIMS profiles of a 17 and 52 Ohm/sq emitter. The colored areas mark the emitters etched back to the same surface concentration of $2x10^{20}$ cm^{-3}.

The etch-back step must be carried out in a very controlled manner, since only a few tens of nanometers must be etched. This can be done even on large area wafers by forming porous silicon in a wet-chemical etching bath and removing the porous silicon afterwards [10]. When etching the above mentioned emitters back to the same [$P_{Surface}$] of $2x10^{20}$ cm^{-3}, the sheet resistance rises from 52 Ohm/sq to 118 Ohm/sq and from 17 Ohm/sq to 73 Ohm/sq respectively. The etch-back step introduces a new parameter to decouple [$P_{Surface}$] and emitter depth in combination with highly doped initial emitter profiles. The performance of the emitter in combination with its surface passivation as used in solar cells can be characterized by measuring the emitter saturation current density j_{oe} by QSSPC (Quasi-Steady-State Photo-Conductance). Floatzone wafers with an emitter and fired PECVD (Plasma-Enhanced Chemical Vapour Deposition) SiN_X:H on both sides are used. Book et. al [9] received the results presented in Fig. 2.

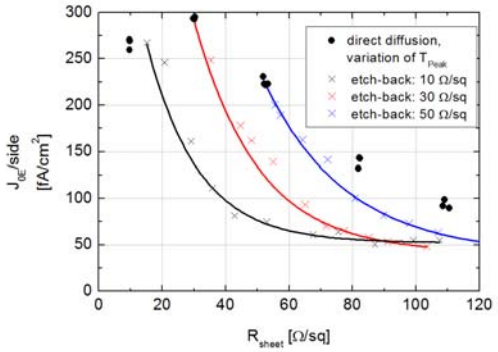

Figure 2 j_{0e} vs. sheet resistance etched back from different heavy $POCl_3$ diffusions [11].

Low j_{oe} values of 50 fA/cm^2 can be reached by etching back a 30 Ohm/sq $POCl_3$ emitter to 90 Ohm/sq. If this emitter is etched back to 65 Ohm/sq, a j_{oe} of 90 fA/cm^2 was measured. To reach the same j_{oe} by a $POCl_3$ diffused emitter without etch-back, the diffusion temperature must be significantly lowered. This leads to a high sheet resistance of 110 Ohm/sq. The etch-back process thus allows low emitter saturation current densities in combination with a sufficiently high lateral conductance in the emitter. A low j_{oe} value in combination with a high lateral conductivity supports the application in a screen printed solar cell process, since rather wide finger distances can be used to minimize shading losses. Furthermore, the complexity on the diffusion side can be reduced when using etch-back emitters. It is easier to form a homogeneous 30 Ohm/sq than a high ohmic 80 Ohm/sq emitter in a $POCl_3$ diffusion over the whole tube length.

2.1 Etch-back solar cell process

The etch-back process can be used to form a selective emitter. This is the preferred method to process high efficiency screen printed solar cells. The high doping level underneath the contacts helps to form a good contact with low contact resistance and widens the process window in the firing step. The process was first published in [10] and can be seen in Fig. 3. After the emitter formation, a mask is printed by either using screen or inkjet printing technique. The etch-back step follows and the mask is removed in a wet-chemical solution. The edge isolation can be done in several ways. The preferred method is to do this by single side etching, after the mask was printed. An inline wet bench can be used that contains all three modules in one system (edge isolation, etch-back and mask removal). The rest of the process is the same as in a standard production line. PECVD SiN_X:H is deposited on the front side as surface passivation and anti reflection coating. The contacts are formed by screen printing Ag paste on the front side and Al paste on the rear. Cofiring is carried out in a belt furnace and forms also the full area Aluminum back surface field.

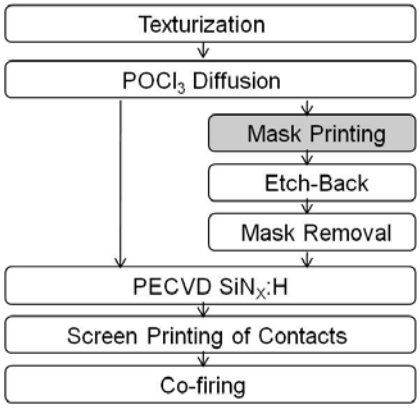

Figure 3 Process scheme for the selective emitter solar cell.

2.2 Reflection properties

The reflection properties of etched-back surfaces were also investigated to quantify possible losses. A limiting factor for using a lower starting sheet resistance may be the increased etch-back depth which affects the surface texture and thus the reflection of the solar cell. SEM images of deeply etched samples were recorded. In Fig. 4 a pyramid after an etch-back of 265 nm can be seen. The valleys of the texture are rounded while the tips remain sharp. Possible reflection losses have their origin in the rounded valleys. Reflection was measured on etched back surfaces of different depth coated with SiN_X:H. The reflection curves were used for the determination of j_{sc} losses using a typical IQE of a selective emitter solar cell [11]. The loss in short circuit current is 0.05 mA/cm^2 if 90 nm of silicon is etched-back and is negligible.

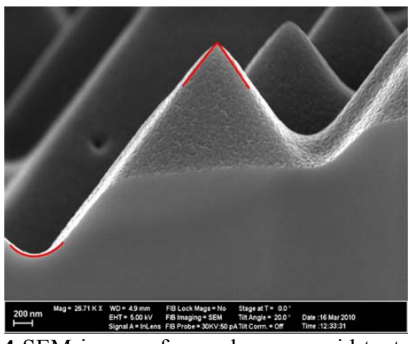

Figure 4 SEM image of a random pyramid textured Cz-Si wafer after removing the 265 nm thick porous layer [11].

2.3 mc-Si silicon and grain boundaries

If mc-Si is used in an etch-back process, grain

boundaries and dislocations may be etched faster and cause problems. SEM images showed no significant preferred etching if 60 nm silicon is removed (Fig. 5). Although the grain boundary is visible from the top, the depth cannot be determined from the cross-section cut by a focused ion beam (FIB).

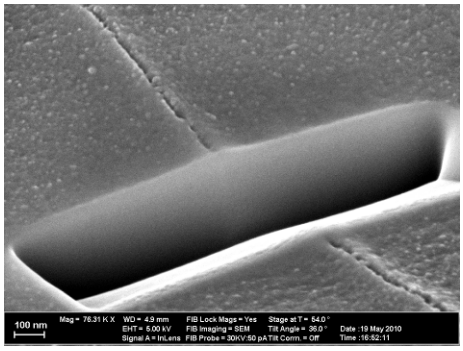

Figure 5 SEM image of a FIB cut at an etch groove after a 60 nm etch-back [11].

On very deeply etched samples (about 220 nm) few grain boundaries can be found with deeply etched grooves. The increased etching rate only occurs at certain crystal orientations at the grain boundary surface [11].

2.4 Solar cell results

First published results [10] using 5 inch Cz-Si wafers with 1.5 Ohmcm resisitivity showed an efficiency increase of 0.3% absolute compared to references with homogeneous emitter. The average efficiency of the selective emitter solar cells was 17.9% and maximum efficiency was 18.1%. The further development led to an efficiency increase of 0.5% absolute compared to references (Tab. I).

Table I: Average IV results of 5 inch Cz-Si solar cells (9 cells per group). Wafer resistivity: 2.8 Ohmcm [12].

	FF [%]	V_{OC} [mV]	j_{sc} [mA/cm^2]	η [%]
Reference	78.1	629	36.9	18.2
Selective Emitter	78.1	639	37.5	18.7

The random pyramid texture was improved as well as the front side metallization, new pastes allow printing narrower fingers with a finger width between 90 and 110 µm. Wafer resistivity was 2.8 Ohmcm. A sheet resistance of 30 Ohm/sq obtained by $POCl_3$ diffusion was used, 65 Ohm/sq was the sheet resistance of the etched-back regions. To obtain the sheet resistance ratio, 60 nm of silicon have to be etched-back. The efficiency of the best selective emitter solar cell from this cell run was confirmed by FhG-ISE CalLab with 18.7% (stable efficiency under illumination).

By changing the initial $POCl_3$ diffusion to 20 Ohm/sq and etching back to 95 Ohm/sq, a maximum efficiency of a selective emitter solar cell was measured to 19.0%. No plating technology or special cleaning steps have been applied.

5 inch mc-Si solar cells were processed using an isotexture at the beginning. Wafers with high and low dislocation and grain boundary density were used. Selective emitter solar cells were diffused with a 30 Ohm/sq emitter. In Tab. II the IV results can be seen.

Table II: Average IV results of 5 inch mc-Si solar cells, high quality wafers [11].

	FF [%]	V_{OC} [mV]	j_{sc} [mA/cm^2]	η [%]
Reference	79.1	612	33.1	16.0
Selective Emitter	78.2	617	34.1	16.5

Low quality wafers resulted in a decrease in fill factor of 1.5% and a loss of 1 mV in V_{OC} compared to the references. The gain in j_{sc} of 0.4 mA/cm^2 could not compensate the other losses. These results suggest to optimize the initial diffusion and etch-back depth.

2.5 n-type solar cells

The etch-back process can be used to process n-type silicon wafers with a highly effective FSF. n-type material does not suffer from the boron-oxygen degradation. The same process as shown in Fig. 3 can be used for n-type material. The emitter in this case is on the rear side and is formed by alloying screen printed aluminum paste. Since the pn-junction is on the rear side, the base material must have a high diffusion length to collect the generated current. 6 inch Cz-Si n-type material with a resistivity of 8 Ohmcm and a thickness of 200 µm was used to process solar cells with uniform and selective FSF in a first test (see also [9] for more details).

Table III: First IV results of 6 inch Cz-Si n-type solar cells. The efficiency gain by the selective FSF is 0.8%.

	FF [%]	V_{OC} [mV]	j_{sc} [mA/cm^2]	η [%]
Uniform FSF	78.6	629	35.5	17.6
Selective FSF	78.7	638	36.6	18.4
Best Selective FSF	78.5	639	36.8	18.5

The sheet resistance for the selective FSF solar cells was 35 Ohm/sq for the highly doped and 100 Ohm/sq for the lowly doped regions respectively. The solar cells with the etched-back FSF show an efficiency gain of 0.8% absolute compared to the reference cells with uniform FSF. The differences in FSF quality can be seen in the spectral response measurement (Fig. 6). A maximum efficiency of 18.5% was achieved. This is to our best knowledge the highest published efficiency for large area screen printed rear junction n-type solar cells. There is still room for improvement due to some front side metallization problems which can be easily solved in further process runs. This emphasizes the highly efficient selective front surface field obtained by the etch-back process. For an industrial application, a possibility to solder the aluminum rear side must be found if conventional module technology should be used. Ag/Al soldering pads on the rear as in standard screen printed p-type solar cells cannot be used. The pads do not form an efficient emitter on the rear on large areas and would produce shunts.

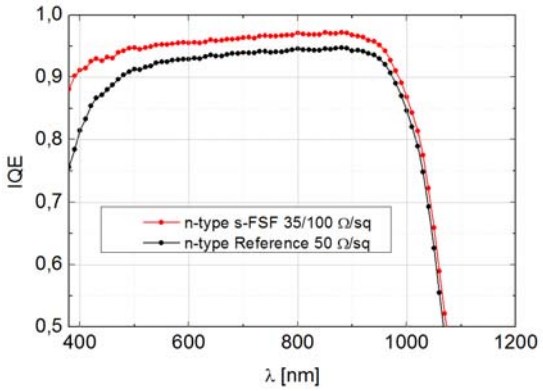

Figure 6 Internal Quantum Efficiency of a 6 inch n-type Cz-Si solar cell with a homogeneous 50 Ohm/sq FSF (black) and a selective FSF (red).

3 SUMMARY

The etch-back process in combination with a masking step is an industrially feasible scheme to form a selective emitter structure on p-type or a selective FSF on n-type wafers. The etch-back process can be realized with high homogeneity on large area wafers by forming porous silicon in a wet-chemical solution and removing the porous silicon afterwards. Etch-back emitters can decouple the emitter saturation current densities and sheet resistances to a certain degree. The phosphorous concentration on the surface can be lowered while the emitter depth is still sufficient to reach a good lateral conductivity. This high efficiency selective emitter is suitable for a screen printing metallization process, and the finger distance can be chosen wide enough to not increase shading losses.

An additional advantage of this process is that it is easier to form a highly doped $POCl_3$ emitter (20 or 40 Ohm/sq) homogeneous over the whole tube length than to form a directly diffused high ohmic emitter. Nevertheless, there is the need for an aligned printing step for the metallization.

The j_{SC} loss by etching-back the texture is negligible. The loss in j_{SC} is 0.05 mA/cm^2 if 90 nm of silicon is removed. A typical etch-back depth is 60 nm.

On mc-Si grain boundaries may be preferentially etched. An adapted initial diffusion and etch-back depth maybe a possibility to have a gain in efficiency even on low quality mc-Si material.

The efficiency gain due to the selective emitter structure was 0.5% absolute on Cz-Si and on high quality mc-Si material. A 5 inch Cz-Si solar cell reached an independently confirmed stabilized efficiency of 18.7% (ISE CalLab). This can be further improved e.g. by changing the initial diffusion to lower values and reducing the width of the printed mask– we measured an efficiency of up to 19.0% using 5 inch Cz-Si and a full area Al back surface field.

The etch-back process can also be used to form a selective FSF on n-type solar cells. A 6 inch solar cell processed from 8 Ohmcm n-type Cz-Si material with a screen printed Al alloyed emitters reached an efficiency of 18.5% in a first test. The gain compared to a uniform FSF was 0.8%. Before this process would be introduced into industry, the problem of soldering aluminum on the rear must be solved if conventional module technology is used. A possible solution was presented by Halm et al. [14]. Alternative designs for the electrode at the module level are also interesting alternatives [15]. The process is very attractive, since no boron-oxygen degradation occurs in n-type silicon and there is no significant change in the solar cell process compared to the selective emitter process using p-type material.

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5 REFERENCES

[1] M. Hörteis et al.: Fundamental Studies on the Front Contact Formation Resulting in a 21% Efficiency Silicon Solar Cell with Printed Rear and Front Contacts. Proc. 35th IEEE PVSC, Hawaii, 2010

[2] H. Antoniadis et al.: All Screen Printed Mass Produced Silicon Ink Selective Emitter Solar Cells , Proc. 35th IEEE PVSC, Hawaii, 2010

[3] A. Esturo-Breton et al.: Crystalline Si Solar Cells with Selective Emitter for Industrial Mass Production, Proc. 24th EPVSEC, Hamburg, 2009

[4] Z. Shi et al.: Mass Production of New High Efficiency Multicrystalline Silicon Solar Cell Technology with Selective Emitter, Proc. 24th EPVSEC, Hamburg, 2009

[5] H.H. Kuehnlein et al.: Next Generation of Front Grid Metallization: LCP Selective Emitter Combined with Ni-Cu-Sn Direct Plating on Silicon, Proc. 24th EPVSEC, Hamburg, 2009

[6] J.R. Köhler et al.: Laser Doped Selective Emitters Yield 0.5% Efficiency Gain, Proc. 24th EPVSEC, Hamburg, 2009

[7] G. Hahn: Status of Selective Emitter Technology, this conference

[8] B. Raabe et al.: Monocrystalline Silicon–Future Cell Concepts, Proc. 22nd EUPVSEC, Milan, 2007

[9] F. Book et al.: Large Area n-Type Silicon Solar Cells with Selective Front Surface Field and Screen Printed Aluminum –Alloyed Emitter, this conference

[10] H. Haverkamp et al.: Minimizing the Electrical Losses at the Front Side: Development of a Selective

Emitter Process from a Single Diffusion, Proc. 33rd IEEE PVSC, San Diego, 2008

[11] F. Book et al.: The Etchback Selective Emitter Technology and its Application to Multicrystalline Silicon, Proc. 35th IEEE PVSC, Hawaii, 2010

[12] F. Book et al.: Detailed Analysis of High Sheet Resistance Emitters for Selectively Doped Silicon Solar Cells, Proc. 24th EPVSEC, Hamburg, 2009

[13] D.L. Meier, H.P. Davis, R.A. Garcia, J. Salami, A. Rohatgi, A. Ebong and P. Doshi, Aluminum alloy back p–n junction dendritic web silicon solar cell, Sol. En. Mat. & Sol. Cells, 65, 2001, 621

[14] A. Halm et al.: 'Low Temperature Pads on Al-Emitter or Al-BSF' Proc. 24th EU PVSEC, Hamburg, 2009, p. 1462

[15] A. Schneider et al.: 'The Day4™Energy Electrode – A New Metallization Approach Towards Higher Solar Cell and Module Efficiency' Proc. 21st EU PVSEC, Dresden, 2006, p. 230