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Influence of Firing Temperature on APCVD Poly-Si Properties for Fired Passivating Contacts

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Abstract. We demonstrate the usage of boron-doped polycrystalline-silicon (poly-Si) fabricated by atmospheric pressure chemical vapor deposition for the formation of fired passivating contacts. Layers of different thicknesses are studied regarding their crystallite size, resistivity, and passivation properties for different fast firing temperatures. From X-ray diffraction measurements, it is concluded quantitatively that a higher firing peak temperature increases the crystallite size of the poly-Si to values up to 10 nm. This change in crystallite size varies inversely proportional with the resistivity, which is drastically decreased for higher firing temperatures. Higher implied open circuit voltages (iV_{OC}) and lower saturation current densities (J_0) are found for thinner poly-Si layers and at higher firing temperatures, most probably due to a difference in hydrogen diffusion time from the SiN_X:H layer to the interface oxide. Although no blisters of the (p) poly-Si are observed, blistering of the SiN_X:H layer at high firing temperatures >900°C impairs the passivation for thin layers. A maximum iV_{OC} of 708 mV and minimum J_0 of ~12 fA/cm^2 are achieved.

INTRODUCTION

Passivating contacts have shown to enable high conversion efficiencies due to their excellent charge carrier selectivity and passivation quality [1]. However, their quality normally relies on an extended annealing step at elevated temperatures, which makes their integration into existing process flows in industry more challenging. In the fired passivating contacts (FPC) approach, crystallization and thus dopant activation is carried out simultaneously within the already existing fast firing step for hydrogenation and metallization [2]. Passivation and poly-Si resistivity for the FPC approach require specific attention. Although a low recombination was already shown [3, 4, 5], one major issue was blistering of the poly-Si during thermal treatment due to a high hydrogen content in the amorphous silicon (a-Si) layer, in case of plasma enhanced chemical vapor deposition (PECVD). This calls for additional measures to be taken such as an annealing step before SiN_X:H deposition [3]. An alternative for a-Si deposition is provided by atmospheric pressure chemical vapor deposition (APCVD), where the poly-Si is less susceptible to blistering due to the difference in deposition method, which has already been show to enable a high passivation quality for the standard high temperature passivating contact (HTPC) [5, 6].

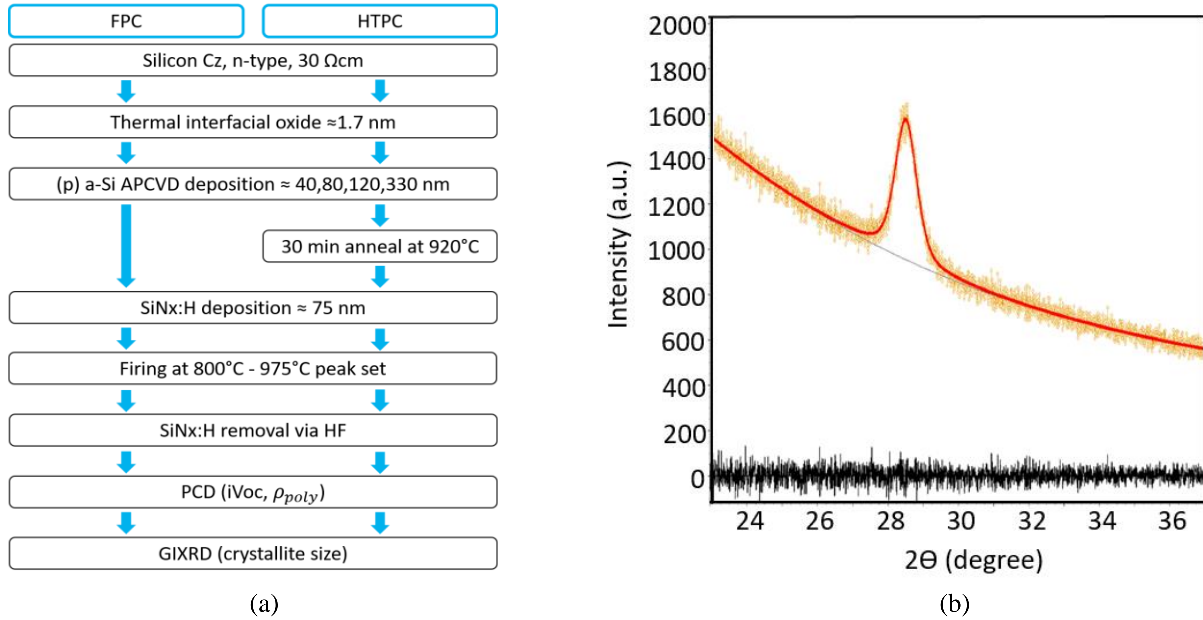
METHODS

The process flow for the experiment is shown in Fig. 1 (a). A thin SiO_X layer (~1.7 nm) was grown by thermal oxidation in a tube furnace onto the phosphorus-doped 30 Ωcm Cz-Si wafers. In the following, boron-doped a-Si was deposited via APCVD on both sides. Different thicknesses of approximately 40, 80, 120 and 330 nm, determined by scanning electron microscopy, were realized by varying the belt speed during deposition. Additionally, reference samples were crystallized in a tube furnace at 920°C to realize the HTPC. For hydrogenation, a ~75 nm thick H-rich SiN_X:H layer was deposited on both sides of all samples using PECVD. The subsequent fast firing in a conventional fast firing belt furnace was performed at set peak firing temperatures between 800 - 975°C, where four samples were used for each firing temperature. For characterization of the crystallite size, the SiN_X:H was removed in 10% HF. A Sinton lifetime tester WCT-120 was used to determine implied open circuit voltages (iV_{OC}) and saturation current

density (J_0) values as well as the poly-Si resistivity with errors being calculated through standard deviation of the individual samples. The validity of resistivity measurements was confirmed via four-point probe measurements for separately prepared samples. X-ray diffraction (XRD) measurements were performed with a Bruker Advance D8 in the grazing incidence method under an incidence angle of $\omega = 1°$ and with a 2.5° Soller slit [7]. The data was recorded between 2Θ values of 20° and 40° with a step size of 0.05°. Evaluation is done via the Rietveld method in the fundamental parameter approach, where a Voigt function is fitted to the silicon diffraction peak at $\Theta \approx 29°$ [8, 9], as is exemplary shown in Fig. 1. (b) The crystallite size D is then calculated via the Debye formula

$$D = \frac{\lambda}{\beta \cos(\theta)} \tag{1}$$

where $\lambda = 0.1542$ nm is the wavelength of the copper anode and β the integrated breadth. This is obtained by dividing the area beneath the fitted Voigt curve by its height.



(a) (b)

FIGURE 1. (a) Process flow for the experiment with FPC and HTPC samples. (b) Exemplary XRD measurement in grazing incidence mode of the (111) silicon peak. The result of a Rietveld refinement is shown with the comparison between measured (yellow dots) and refined pattern (red line). The difference between the collected and refined patterns (black line) is flat over the whole measured range. For every refinement a polynomial background is subtracted (grey line).

RESULTS

The poly-Si resistivity in Fig. 2 (a) decreases by one order of magnitude for higher firing temperatures. For the thickest poly-Si layer, the resistivity is reduced significantly for all firing temperatures. This could probably be due to the longer deposition time at 650°C allowing for more boron atoms to be arranged substitutionally on Si lattice sites. A significant rise in crystallite size for temperatures ≥850°C is visible in Fig. 2 (b), while below that temperature the samples are almost completely amorphous. A similar sharp increase in crystallinity at 850°C is also observed in Raman measurements. A trend for continuously increasing crystallite sizes with temperature is observed for higher firing temperatures above 850°C. The crystallite sizes are even larger for the HTPC samples for which the annealing duration is much longer. However, the difference in crystallite size between HTPC and FPC is reduced for the thinnest layer compared to thicker ones. Moreover, a thicker layer generally corresponds to larger crystallites, which holds especially for the HTPC samples.

The changing resistivity could be related to the varying crystallite size. More grain boundaries lead to more charge carriers being trapped due to the emerging potential barrier, which is especially true for a high doping concentration [11]. In Fig. 3 (a), the poly-Si resistivity is shown in dependence of the crystallite size for different poly-Si thicknesses. Fits are performed according to an inverse proportionality between crystallite size and resistivity with an additional proportionality constant [12]. The overall agreement suggests that the observed change in resistivity during firing is in fact mainly induced through the evolution of the crystallite size towards higher firing temperatures. The crystallization process leads to more boron being incorporated into the lattice sites, which then induces stronger band bending in the Si wafer and in turn improves the passivation quality.

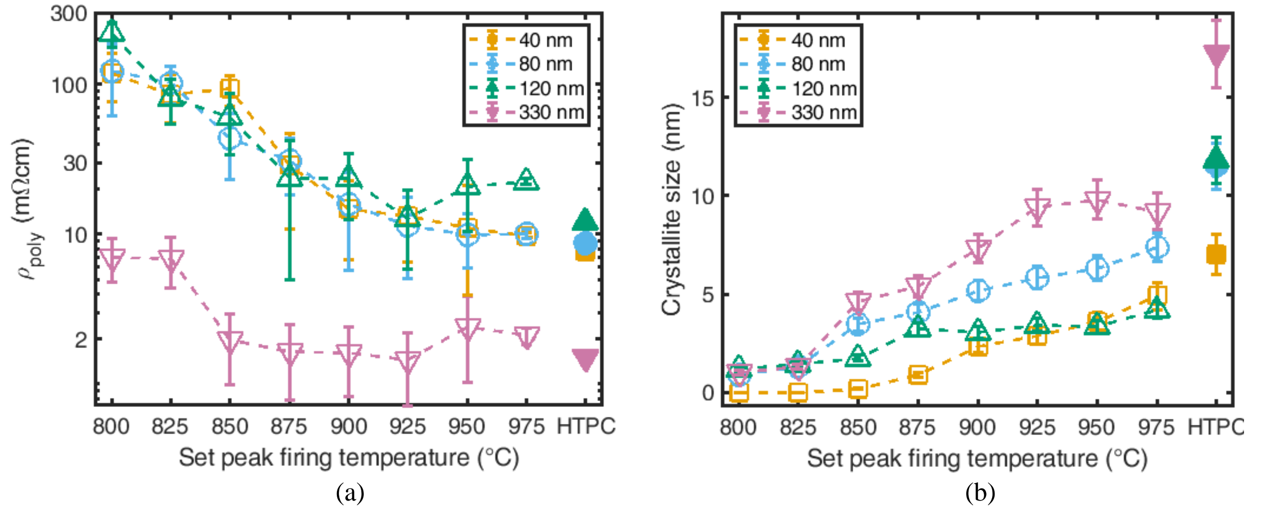


FIGURE 2. (a) Poly-Si resistivity and (b) crystallite size for different set peak firing temperatures and HTPC reference samples after SiN_X:H removal.

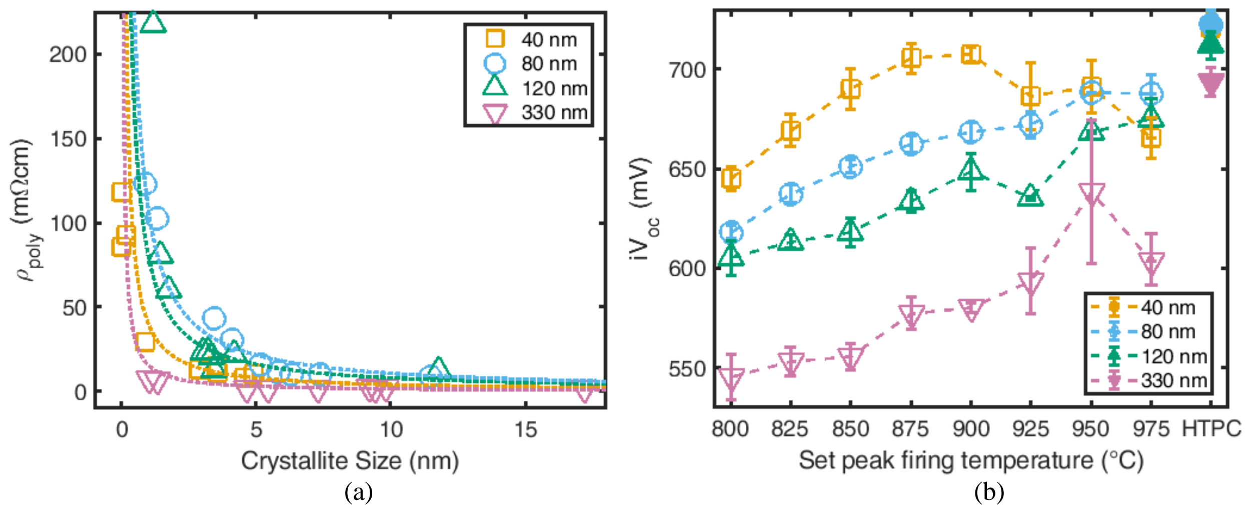


FIGURE 3. (a) Poly-Si resistivity in dependence of the crystallite size. Fits are obtained through an inverse proportionality. (b) iV_{OC} values for different (p) poly-Si thicknesses after fast firing in dependence of the set peak firing temperature, and HTPC samples, that were fired with a fixed temperature profile.

In Fig. 3 (b), the relation between iV_{OC} values and firing temperature is shown after fast firing. A thicker layer leads to a lower iV_{OC}, most probably due to the longer time needed for hydrogen to diffuse from the SiN_X:H to the poly-Si/SiO_X interface. Generally, a higher firing temperature corresponds to a higher iV_{OC}. This could be due to larger amounts of hydrogen being released during firing at higher temperatures to passivate the grain boundaries and the poly-Si/SiO_X interface. The deviation of this trend for the thinnest layer at temperatures above 900°C can be attributed to blistering of the SiN_X:H layer. This further supports the argument of a decreased hydrogen diffusion time to the poly-Si/SiO_X interface for thinner poly-Si layers, as a higher density of hydrogen atoms could then be accumulated within thinner poly-Si layers during firing. Those hydrogen atoms can then rapidly effuse during high temperature firing, leading to blistering [2]. A maximum iV_{OC} of 708 mV and minimum J_0 of 12 fA/cm^2 is found at 900°C for the FPC for the thinnest poly-Si layer.

CONCLUSION

Contrary to PECVD poly-Si, the lack of poly-Si blisters for APCVD enables the usage of only one high temperature (firing) step after SiN_X:H deposition. We demonstrate the effect of firing temperature on in-situ-doped (p) a-Si layers with different thicknesses using an APCVD in-line tool from Schmid Thermal Systems. PCD measurements are used to extract the poly-Si resistivity. Hereby, a decreasing resistivity for higher firing temperatures is observed. XRD measurements show that firing at higher temperatures leads to larger crystallite sizes for all thicknesses. An activation temperature of at least 850°C (set peak temperature) is required for this effect to be detected. This is more pronounced for thicker a-Si layers compared to thinner ones. It is demonstrated that the changes in crystallite size and poly-Si resistivity are firing-induced, as they are inversely proportional to one another. After firing

for hydrogenation, the passivation in terms of iV_{OC} increases up to 708 mV with a J_0 of 12 fA/cm^2 for the thinnest layer and decreases for thicker layers. This is most likely due to more hydrogen being released at higher firing temperatures and presumably longer time for hydrogen to diffuse from the SiN_X:H to the poly-Si/SiO_X interface. For thin a-Si layers, further improvement is currently limited by blistering of the SiN_X:H layers.

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