HIGH EFFICIENCY BURIED CONTACT SOLAR CELLS ON MULTI-CRYSTALLINE SILICON: AN INDUSTRIAL REALITY

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ABSTRACT: This paper reports on the development of an industrially feasible sequence for the production of high efficiency, buried contact solar cells on multi-crystalline silicon. The work builds on a hybrid screen print / buried contact process, which has resulted in excellent solar cell efficiencies using large area multi-crystalline silicon. There are two important aspects to this work. The first is the "industrialisation" of the existing hybrid process, namely a cell process that, unlike the existing process, does not involve a removal of excess screen printed aluminium in hydrochloric acid and the subsequent production of large quantities of a hydrochloric acid / aluminium slurry. The second aspect is the application of an isotexturing technique to this buried contact process. We processed 111 large area (12×12 cm^2) cells and achieved an average cell efficiency of 16.2% and a maximum of 16.9%. The best cell had a V_{oc} of 616 mV, a J_{sc} of 35.0 mA/cm^2 and a fill factor of 78.3%.
Keywords: Buried Contacts, Multi-Crystalline, Screen Printing

1 INTRODUCTION

Multi-crystalline silicon maintains a significant cost advantage over single crystalline silicon. Whereas single-crystalline silicon solar cells are produced commercially using various techniques, production of multi-crystalline silicon solar cells is currently confined to screen printed processes. As yet, therefore, commercial production of buried contact solar cells on multi-crystalline silicon has not been achieved. This paper is based on work progressing in this direction. In order to achieve high efficiency cell results it is necessary to have good front surface texturing and that an industrial process be proven for commercial cell manufacture. The work described in this paper was concerned with the application of an isotexturing technique to buried contact cell design and with improvement of an existing process to produce a more industrially-friendly processing technique.

The term "buried contact" was perhaps first coined by Federico Faggin, who, in 1968, invented a very different sort of buried contact, which was subsequently used in the first single-chip microprocessor – the Intel4004 [1]. Buried contact solar cells were developed and patented by Wenham and Green at the University of New South Wales in the 1980s [2]. Mono-crystalline silicon buried contact (Saturn) cells on single crystalline silicon have been, and continue to be, produced commercially in high volume by BP Solar at its facilities in Spain - over 80 MWp have been produced since 1992.

Figure 1 shows the structure of the hybrid screen print / buried contact solar cell used in this work. Like most buried contact designs, this scheme has the advantages of a selective emitter, reduced shading losses due to the buried grid and an increased contact area between the emitter and the metal. In addition, this design includes a screen printed aluminium rear. This results in a very thick back surface field and possibly in additional gettering, both beneficial for multi-crystalline silicon.

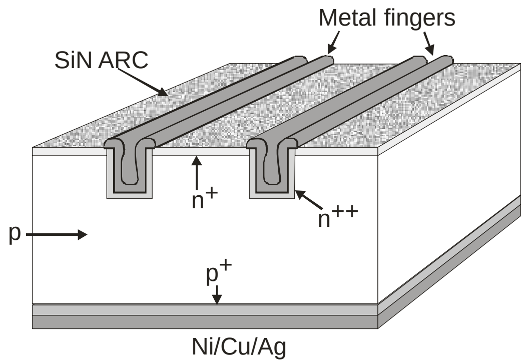

Figure 1: Design of the hybrid screen print / buried contact solar cell. The front surface has a SiN anti-reflection coating and is isotextured. There is a light phosphorous diffusion over the full front surface and a heavy phosphorous diffusion in the grooves. The rear side has a screen-printed aluminium back surface field. The metallisation is done using an electroless plating bath with Ni, Cu and Ag.

The purpose of the work described in this paper was twofold, namely the "industrialisation" of the hybrid screen print / buried contact process and the application of isotexturing to the new process. A large number of cells (111) across a full brick were processed to determine the suitability of this process.

2 BACKGROUND

The hybrid screen print / buried contact process, as existed prior to this work, and isotexturing, which was applied to the cells made in this work, are described in more detail below.

2.1 Hybrid Buried Contact / Screen Printed Process

The hybrid screen print / buried contact process was developed by W. Jooss et al. [3] and has resulted in excellent efficiencies on multi-crystalline silicon, including a world record for large area cells [4]. This process includes a selective emitter and a silicon nitride anti-reflection coating. The record efficiency cell was obtained with a mechanically V-textured front surface, providing excellent light trapping. A thick back surface field is formed by screen printing and firing of an aluminium layer. After firing, the excess aluminium is removed from the rear of the wafer, typically in a hydrochloric acid solution. The front contact grid and full rear are then metalised using Ni and Cu plating. In the case of the record efficiency cell, there was also a 2 µm thick evaporated aluminium layer between the BSF and the Ni.

The disadvantage of this process is that removal of the excess aluminium results in large quantities of hydrochloric acid / aluminium paste slurry that must be disposed or filtered for reuse, but is necessary because the screen printed aluminium does not withstand the plating solutions. The existing hybrid process is therefore not particularly suited to industrial production.

2.2 Isotexturing

Industrial-scale texturing of single-crystalline silicon has become a standard process that, unfortunately, does not transfer well to multi-crystalline silicon. The different grain orientations found in multi-crystalline silicon mean that alkaline or anisotropic texturing cannot be used. Many groups have developed solutions containing HF, HNO_3 and organic additives [5, 6]. At the University of Konstanz, a method and solution have been developed that results in excellent surface texture, yet that consists only of HF, HNO_3 and H_2O [7]. This method provides simultaneous saw damage removal and surface texture.

The primary reason for texturing is to reduce reflection from the front side of the wafer. The more homogeneous appearance can also be of advantage in applications where the aesthetics of the solar cell is important. Figure 2 shows the reflectance from a wafer etched in a standard alkaline solution, compared with that from an isotextured wafer. Both wafers were multi-crystalline silicon and the total reflection was reduced from 36.0% for the alkaline etched wafer to 23.4% for the isotextured wafer.

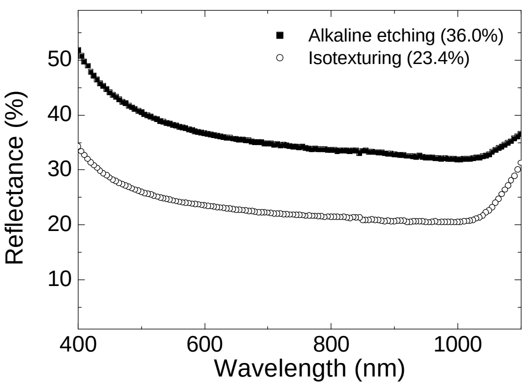

Figure 2: Reflectance curves comparing alkaline etched and isotextured wafers. The total reflection was 36.0% for the alkaline etched wafer and 23.4% for the isotextured wafer.

At the University of Konstanz, an inline isotexturing system has been developed together with the company RENA. This system is capable of texturing 500 12.5×12.5 cm^2 wafers / hour and occupies only 8 m^2 of floor space. Recent results from this system are presented elsewhere at this conference [8].

3 CELL PROCESSING

In order to avoid the need for the hydrochloric acid etch (to remove excess aluminium prior to plating) and thereby "industrialise" the existing hybrid process, a modified process was developed, the results of which are described in this paper. A total of 111 cells of size 12×12 cm^2, taken from the inner region of a BP Solar HEM ingot were processed. The wafers were selected so as to sample the full height range of the brick.

Processing was shared between the University of Konstanz and the BP Solar facilities in Sunbury-on-Thames. The cells were first isotextured at the University of Konstanz, shipped to BP Solar for the front end processing and then returned to the University of Konstanz for aluminium printing, firing and final metallisation. A schematic of the process is shown in Figure 3.

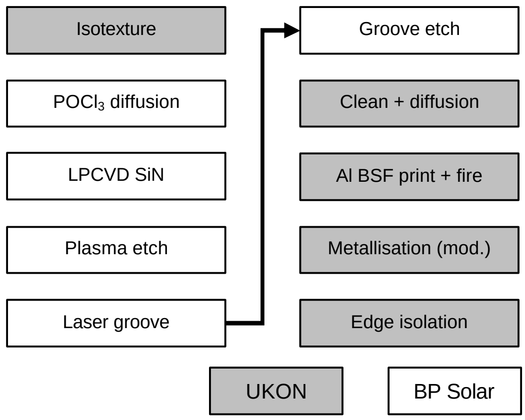

Figure 3: Schematic of the processing used for the cells presented in this work. The shaded steps were done at the University of Konstanz, and the remainder at the BP Solar facilities in Sunbury-on-Thames.

4 CELL RESULTS

To the best of our knowledge, this was the first time that isotexturing was combined with buried contacts. Figure 4 shows an SEM picture of a buried contact groove on an isotextured wafer. The groove was metallised using electroless plating of Ni and Cu.

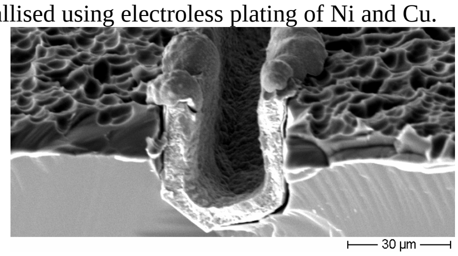

Figure 4: SEM image showing an isotextured wafer with a metallised (Ni and Cu, no Ag) groove

Figures 5 and 6 show J_{sc}, V_{oc}, FF and efficiency values as a function of position for the 111 cells. There is a relatively large variation in fill factor for a given position, due to variations in the electroless plating. The variation in the relevant electronic properties of the material after processing over the full brick is quite small, as indicated by the relatively small variation in J_{sc} and V_{oc}. One disadvantage of the “industrialised” process is that it does not include a bulk hydrogenation step. In the standard hybrid process this is done using Microwave Induced Remote Hydrogen Plasma, MIRHP, after removal of the excess screen printed aluminium and prior to metallisation. The hydrogenation typically has a greater effect on the worst cells, thus the influence of brick position on final efficiency would be expected to be further reduced if a hydrogenation step, such as MIRHP, or the firing-through of SiN that occurs in standard screen print processing, was introduced.

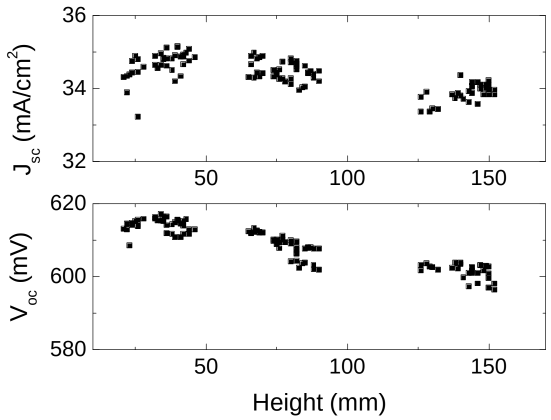

Figure 5: J_{sc} and V_{oc} values for the 111 cells processed in this work as a function of vertical position in the brick. The high J_{sc} values are attributable to the low front surface reflection as a result of the isotexturing. The good quality of the material is evident in the V_{oc} values.

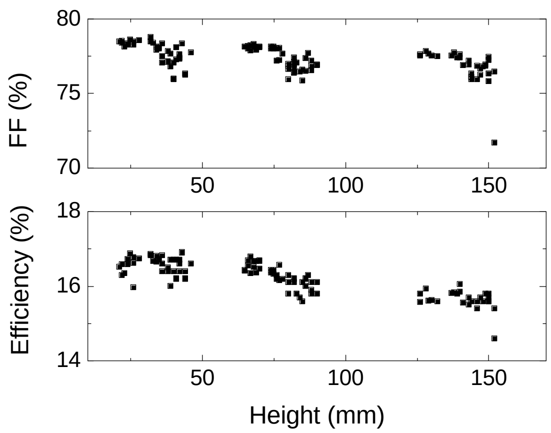

Figure 6: FF and efficiency values for the 111 cells processed in this work as a function of vertical position in the brick.

The average efficiency of all cells was 16.2%. Slightly more cells were processed from the lower (better) positions, and the position-weighted average efficiency is 16.1%. Average IV data and those for the best cell are given in Table I.

Table I: IV data for the best cell and for the average of the 111 cells.

	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	h (%)
Best cell	616	35.0	78.3	16.9
Average (111 cells)	609	34.4	77.3	16.2

Figure 7 shows the IQE curves for two cells, taken from a brick height of 140 mm and 77 mm. Also shown is the reflectance curve for the cell at a brick height of 77 mm. The cell taken from a brick height of 140 mm had an efficiency of 16.1%, which is very close to the group average of 16.2%. The cell from a brick height of 77 mm had an efficiency of 16.6%, which is towards the top end for the cells processed in this work. Both cells have a very good short wavelength response, due to the selective emitter structure and low reflectance due to the isotextured front surface. The main difference in the cells is seen with longer wavelengths, where the cell from the lower brick position clearly has a higher IQE. This is also reflected in the higher V_{oc} (611 mV compared to 603 mV) and slightly higher J_{sc} (34.7 mA/cm^2 compared to 34.4 mA/cm^2) values.

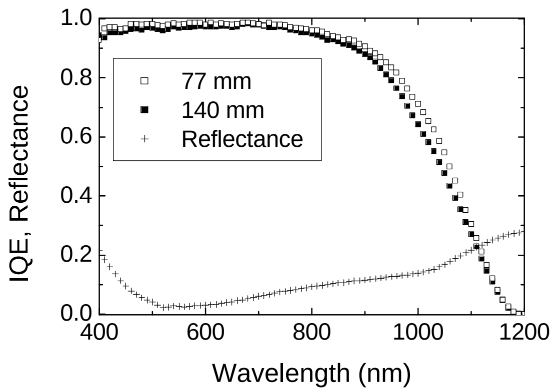

Figure 7: IQE for two cells; taken from a brick height of 140 mm (filled squares) and 77 mm (open squares). The reflectance curves for the two cells were very similar and the reflectance curve for the cell taken from a brick height of 77 mm is shown here.

5 COMPARISON WITH STANDARD PROCESS

As a comparison to the new process (process II), the standard, laser grooved buried contact process (process I) was applied to multi-crystalline silicon without isotexturing. Figure 8 shows the results obtained using the two processes. For process I, wafers were taken from different positions in several ingots. For process II, wafers were taken from the inner region of an equivalent ingot.

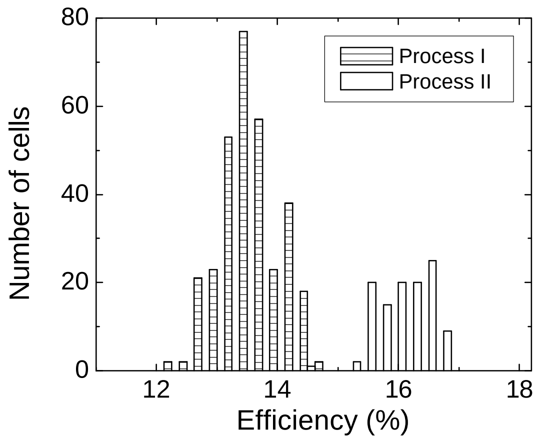

Figure 8: Efficiency histogram comparing the two cell processing techniques. Process I was the standard buried contact process optimised for single crystalline silicon and applied to multi-crystalline silicon. Process II includes isotexturing and an "industrialised" hybrid buried contact/screen print process.

It is clear from Figure 8 that the buried contact process as applied to single-crystalline silicon is not optimised for multi-crystalline silicon. In part, this is due to the front surface texture. Process II cells have an isotextured front surface and process I cells only a standard alkaline etch for front surface texture. The thicker BSF of the process II cells would also contribute to the improved efficiency. In process I, an aluminium layer is sputtered onto the rear and sintered prior to the heavy groove diffusion. This results in only a very thin BSF, typically sub-micron compared to the approximately 7 µm that typically results from our screen printed and fired BSF. The position-weighted averaged IV data for the process II cells and process I cells from a comparable position in the brick are given in Table II.

Table II: Averaged and best results for process I and process II cells from comparable ingot positions.

	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	h (%)
Process I average	586	30.5	76.5	13.6
Process II average	609	34.4	77.3	16.2
Process I best cell	595	31.4	77.5	14.5
Process II best cell	616	35.0	78.3	16.9

6 SUMMARY

We have demonstrated an industrially feasible processing sequence for buried contact solar cells on multi-crystalline silicon. This process avoids the use of an etch in hydrochloric acid, typically done in the hybrid screen printed / buried contact process to remove excess aluminium after the screen print and fire but before the electroless plating. In addition, isotexturing was applied to buried contact cells made using this process. The result was high efficiency cells: 111 12×12 cm^2 cells were processed and the average efficiency was 16.2%, the maximum 16.9%. The best cell had a V_{oc} of 616 mV, a J_{sc} of 35.0 mA/cm^2 and a fill factor of 78.3%. When compared to a process optimised for single-crystalline silicon, and applied to comparable material, the average efficiency was improved from 13.4% to 16.2% and the maximum from 14.5% to 16.9%.

7 ACKNOWLEDGEMENTS

We would like to thank Annette Helfricht and Nidia Gawehns for processing help in the laboratory, Thomas Pernau for LBIC measurements, Wolfgang Jooss for helpful discussions and Kati Huebener, Philip Johnson, Shimir Patel, Richard Snelgrove and Loic Ledernez for cell processing at BP Solar.

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