FUTURE CELL CONCEPTS FOR MC SOLAR GRADE SILICON FEEDSTOCK MATERIAL

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ABSTRACT: The purpose of the work is the investigation of different cell concepts for the newly developed solar grade silicon feedstock (Elkem SoG-Si) from a metallurgical process route, with cost effective refining steps during purification of the silicon. Previous work demonstrated that a standard industrial screen printing process could be adapted to SoG-Si with slight process variation [1, 2]. On large area mc SoG-Si solar cells (156 cm²) efficiencies above 16 % have been demonstrated on an industrial process and confirmed that the SoG-Si is competitive to other PV grade silicon sources. The potential of the SoG-Si material was demonstrated by processing lab-type solar cells with a photolithography based cell process, reaching efficiencies above 18 % on 2x2 cm² [3]. Both cell concepts benefits from the gettering during Al alloying, while future cell concepts have to manage without an Al BSF. For example for very thin wafers. Therefore our bifacial cell concept [4] with a boron back surface field (BSF) was investigated on Elkem SoG-Si.
Keywords: Multi-Crystalline Silicon, Solar Grade, Bifacial

1 ELKEM SOLAR SILICON TECHNOLOGY

The SoG-Si technology has been reported in [1, 2]. As illustrated in Table I, commercial metallurgical grade silicon melt from Elkem's electric arc furnace was treated with pyro- and hydro-metallurgical refining processes including slag treatment, alloying and leaching. The resulting solar grade silicon crystals are melted and further refined before crushing and sizing to suit ingot preparation in the following step.

The energy consumption is calculated to be about 25-30 kWh/kg [1] feedstock material for large scale production. Different processes, which are summarized in Figure 1 were investigated and adapted to the Elkem mc SoG silicon.

Table I: Metallurgical refining process

Process step	**Description**
Elkem Silicon Metal	Elkem Silicon arc furnace
Pyro-metallurgical refining	Energy efficient slag refining
Hydro-metallurgical refining	Acid/Aklkaline surface treatment
Final polishing	Adapting material to customer specific.
	Process exclusively designed for PV Solar manufacturers

2 EFFICIENCY POTENTIAL OF THE SOLAR GRADE MATERIAL

To evaluate the efficiency potential of SoG silicon, lab-type solar cells have been processed on this material. The process is shown in Figure 1 and is discussed in detail in [3]. Using a photolithography based cell process suitable for multicrystalline silicon wafers, SoG-Si solar cells are already close to the efficiency limit of this process determined with floatzone (FZ) reference wafers. FZ solar cells (0.75 Ωcm, 220 µm) showed efficiencies up to η=18.5 % using this process. According to this process four 2x2 cm^2 solar cells (Figure 2) were processed on wafers out of 100% SoG-Si feedstock from Elkem (200 µm).

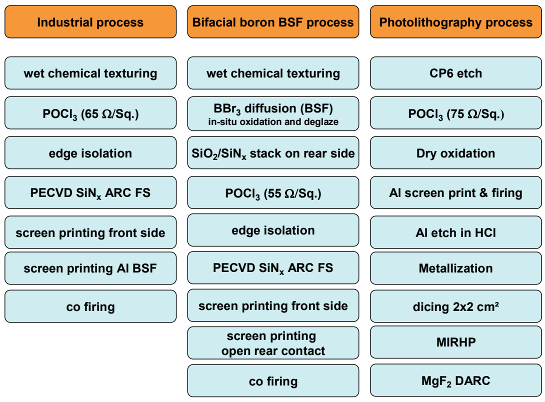

Figure 1: Overview of the different solar cell processes discussed in this paper

The best cell reached an efficiency of stabilized 18.1 % (independently confirmed) with an average >18 % over 4 cells (untextured surfaces, double layer antireflection coating, 75 Ω/Sq $POCl_3$ emitter). This means that the applied process is not sensitive enough to evaluate the ultimate limit of this SoG Si material. An additional benefit is expected if a front surface texture and a local back-surface-field (BSF) instead of the full rear Al-BSF is applied. The solar cell results are summarized in table II.

Table II: Solar cell results on 20x20 mm² cells

Best cell 100% SoG Si	**V_{oc} [mV]**	**j_{sc} [mA/cm²]**	**FF [%]**	**η [%]**
confirmed@ISE	641	35.1	80.3	18.1
UKN	642	35.3	80.3	18.2
10 min@200°C	644	35.6	80.5	18.5
850 min@1 sun	642	35.2	80.5	18.2
0.8 Ωcm FZ (reference)	638	36.0	80.4	18.5

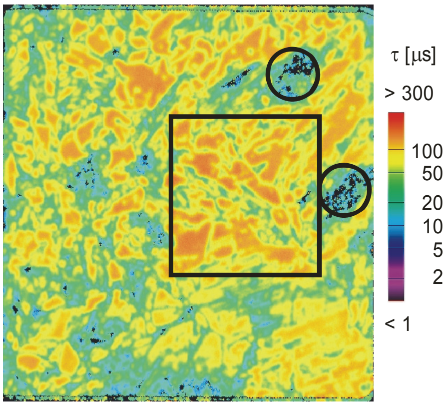

Figure 2: Bulk lifetime mapping of a 125x125 mm² silicon wafer from 100% SoG feedstock. Efficiencies η>16% have been reached on those full size wafers with the industry process while the 50x50 mm² wafer for the lab-type solar cell process is originating from the marked square. Areas of lower quality (black circles) could not be measured reliably with the used measurement setup [3].

3 INDUSTRIAL SOLAR CELL PROCESS

Solar cell results on multi-crystalline wafers with a size of 125x125 mm² and different fractions of solar grade silicon were presented earlier [4]. The cell efficiencies above 16 % were reached on SoG-Si (Figure 3) and proved that the new material is comparable to EG-Si. To reduce costs per W_{peak} the industry also demands for thinner and larger wafer. Therefore wafers of 156x156 mm² size and a thickness of 230 µm were fabricated from 50% SoG-Si and 50% EG-Si. Solar cells were made with our standard industry type process (isotexture, $POCl_3$ diffusion, screen printing metallization, cofiring). The process is shown in Figure 1.

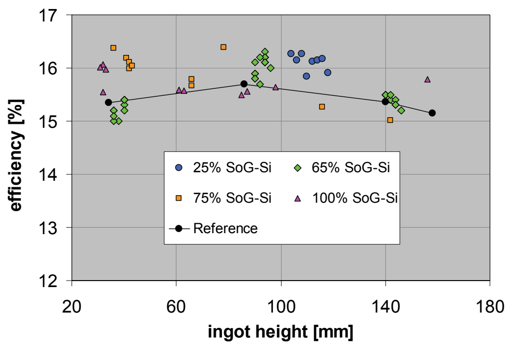

Figure 3: Solar cells results on 125x125 mm² wafers as presented earlier [4]

The solar cell results are shown in table III and Figure 5. The mean values are from wafers of all ingots positions. Two different front side finger grids where used, one standard design with a finger width of 100 µm and one with trapeze like fingers which have a greater width near the busbar and smaller away from the busbar. The open circuit voltage of the solar cell depends on the position of the wafer in the ingot and is plotted in Figure 4. Therefore the solar cell efficiency is also dependant on the brick position.

Table III: Solar cell results on mc SoG-Si 156x156 mm² wafers

	FF [%]	J_{SC} [mA/cm^2]	V_{OC} [mV]	ETA [%]
Trapeze finger Best cell	77.3	33.1	616	15.8
Standard finger Best cell	76.2	33.2	615	15.6
Mean value All wafers	75.6	32.9	611	15.2

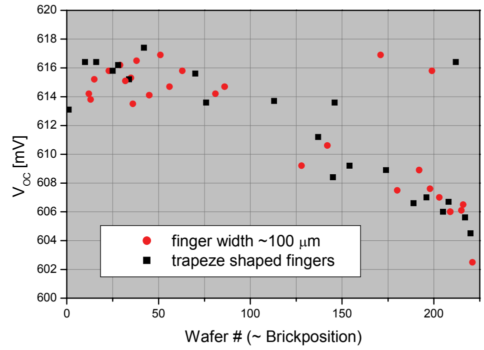

Figure 4: Open circuit voltage as a function of brick position for 156x156 mm² wafers

The cell results are decreased compared to those achieved earlier on smaller wafers. One reason to explain this is the higher series resistance due to the longer length of the fingers on the front side which leads to smaller fill factors. One way to increase the fill factor is to add an additional third bus bar. The first preliminary results showed an increase in fill factor of approx. 1 % absolute, but the J_{SC} couldn't be determined exactly at the moment due to a missing reference for the IV curve measurement in the same design.

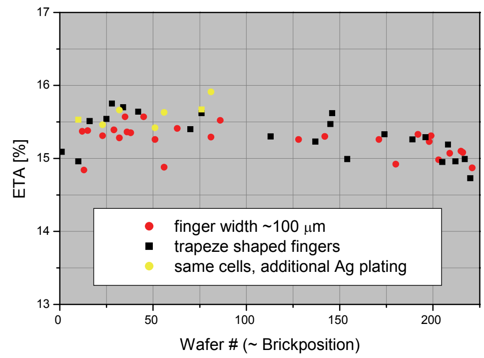

Figure 5: Solar cell efficiencies as a function of brick postion for 156x156 mm² wafers

Another way of reducing R_S is silver plating after the co firing step. This however is an additional process step. The improvement of the cell performance is plotted in Figure 5 (yellow dots) and shown in table IV for the best cell. This indicates that the series resistance in fingers is one of the main factors that decrease performance when processing wafers larger then 156 cm². Therefore screen printing pastes with a higher conductivity are needed.

Tabele IV: Improvement in efficiency and R_S after silver plating for one solar cell

	FF [%]	J_{SC} [mA/cm^2]	R_S [Ωcm²]	ETA [%]
Before plating	75.7	32.8	0.74	15.3
After plating	78.9	32.6	0.37	15.9
gain	+4%	-0.6%	-50%	+4%

New encapsulation techniques using small wires instead of busbars also lead to better fill factors and less series resistance [5] and are therefore beneficial for larger wafers.

4 BIFACIAL BORON BSF SOLAR CELL PROCESS

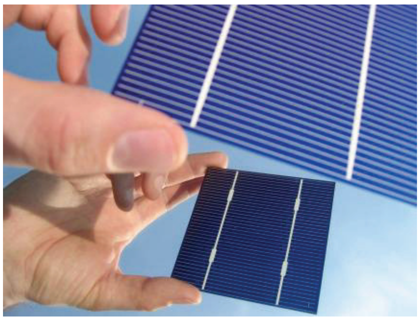

Figure 6: The boron BSF bifacial solar cell. The back side can be seen in the mirror and looks similar to front side

A promising future cell concept for mc silicon is a bifacial design with boron BSF and open rear contact [6], [7]. This process was adapted to mc SoG Si material (mix of 75% SoG and 25% EG Si). Wafer bowing is completely avoided with this process (230 µm thick wafers). The bifacial boron BSF solar cell is shown in Figure 6 and a cross-section in Figure 7. Compared to a standard screen printed solar cell the Al on the back side is missing and cell looks the same from both sides. The process sequence is shown in Figure 1 and is discussed in detail in [6] and [7]. Wafers with 65 % and 75 % SoG Si were used.

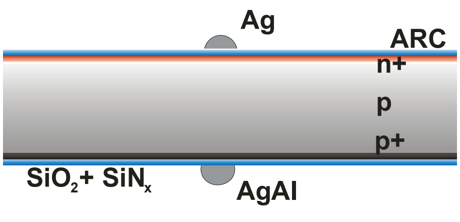

Figure 7: Cross-section of the boron BSF solar cell.

The solar cell results (100 x 100 mm² p-type mc-Si wafer) for the best cells are summarized in table V.

Table V: Solar cell results on 100 x 100 mm² SoG wafers, best cells

	FF [%]	J_{SC} [mA/cm^2]	V_{OC} [mV]	ETA [%]	ratio [%]
75% SoG & 25% EG Si, 230 µm thick					
front side illumination	75.6	34.3	620	16.1	0.77
back side illumination	74.8	26.9	615	12.4	
65% SoG & 25% EG Si, 270 µm thick					
front side illumination	74.9	33.2	618	15.4	0.64
back side illumination	75.2	21.7	609	9.9	

To make further estimations of the cell performance under double sided illumination, the boron BSF solar cell was simulated using PC1D. First the PC1D parameters were fitted to the cell results for illumination from each side separately. With those parameters we simulated the cell performance with one sun illumination on the front side and different albedos on the back side for different wafer thicknesses. The simulated results are summarized in Figure 8. The simulation showed that the increase in wafer performance is expected to be even higher if thinner wafers are considered.

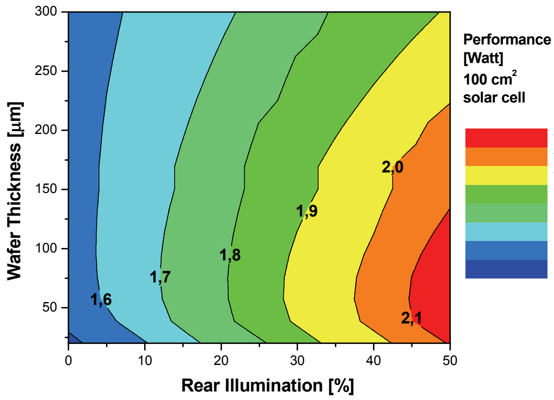

Figure 8: PC1D simulation of the cell performance with different albedos and wafer thicknesses for cell with a thickness of 200 µm, η=15.4 % and back to front ratio of 0.66.

In a preliminary experiment our module was mounted south with an angle of 30°, approx. 50cm above the ground, similar to conventional rack system. The cell was surrounded with a 0.5x1m² black, wooden plate to simulate the shadowing produced by a commercial size panel and a 1.6x1.2 m² white board was placed on the ground to simulate a high reflecting surface as proposed by [8]. A complete IV curve was measured every 20 minutes on a sunny day in mid April with little clouds in the sky. Due to the thin wispy cirrus clouds the irradiation varies. The output power is plotted for monofacial and bifacial illumination in Figure 9.

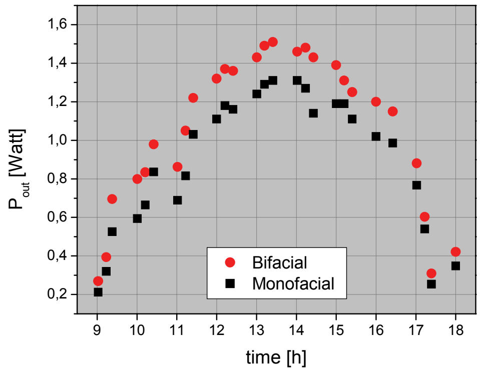

Figure 9: Output power measured over one day in mid April

As expected there is a peak during mid day. The gain due to collecting the albedo on the back side is between 10 % and 35%. It is highest in the morning hours and decreased at mid day. In the afternoon the sky was bit cloudier, also the temperatures of the module increased up to 32° C. Over the day the average gain in performance of the bifacial cell was 19.5 % due to collecting the albedo. For comparison, to improve the output power about 20% of a monofacial mc module with an cell efficiency of 15% the solar cell efficiency has to climb up to 18%.

The albedo could be further increased by using a larger surface with a higher reflection behind the module, for example mirrors could be mounted or small parabolic concentrators. Or small spaces could be left between the solar cells within the module as suggested by [9].

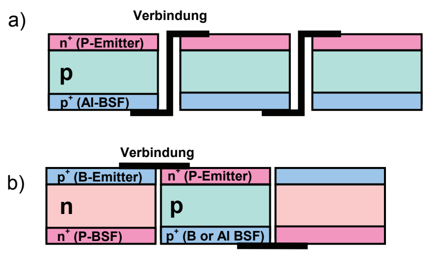

Figure 10: a) Classic module interconnection, each cell backside is connected with the front side of the subsequent solar cell b) alternative module inter-connection using alternating p-type and n-type solar cells [10]

Another benefit of the process is, that is also applicable for n-type wafers. With both cells made from p- and n-type wafer alternative module interconnection is possible [10], with the advantage that the cells could be packed closer together and the flipping of the cells during the tabbing process is not necessary any more.

5 CONCLUSION

It was demonstrated that Elkem mc SoG-Si is applicable in a standard industrial process and is competitive to other PV grade material. The limits of the material are not yet reached by our lab scale process, which gives motivation to apply further process improvements. SoG-Si can keep up with future cell concepts. The bifacial Boron BSF cell concept was successfully implemented on mc SoG-Si material, leading to cell efficiencies exceeding 16% and an expected gain in performance of 20% by using a bifacial module installation.

6 OUTLOOK

The very promising results with the photolithography process on the SoG-Si material give motivation to apply an improved solar cell process on this material. The process for industrial type cells will be further improved. Especially reduced fill factors and series resistances on large area cells are independent on the feedstock source and subject for further investigation. The bifacial process shows a high potential for reducing costs per W_{peak}, not only for SoG-Si but also for n-type silicon and other materials. Therefore efforts are going on upscaling the process and transfering it to the industry.

7 ACKNOWLEDGEMENTS

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