MONOCRYSTALLINE SILICON – FUTURE CELL CONCEPTS

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ABSTRACT: An overview of currently used cell processes for monocrystalline silicon in industry is given. Since the screen printed solar cell process has the biggest market share, advanced screen printing processes are presented. The front-side with selective emitter structures are investigated by measuring the emitter saturation current (j_{0e}) on symmetrical test samples with QSSPC. The reference sample with an industrial homogeneous 50 Ω/□ emitter and fired PECVD SiN has a j_{0e} of 220 fA/cm^2. On selective emitter structures with two diffusion steps, using first a 100 Ω/□ diffusion then a SiN layer as mask and finally a 10 Ω/□ diffusion, j_{0e} is 140 fA/cm^2 using PECVD SiN and 120 fA/cm^2 respectively with LPCVD SiN. By changing the sequence of light and heavy diffusion and applying PECVD SiN for surface passivation, j_{0e} was measured to 90 fA/cm^2. Solar cells were made with a two step selective emitter and a simplified process with a single diffusion step using laser structured SiN as diffusion suppressing layer and no texture was applied to these cells. The best reference cell with homogeneous 50 Ω/□ emitter has an efficiency of 16.2% and 625 mV V_{OC}. The best selective emitter solar cells with both used processes have a 10 mV increase of V_{OC} leading to 635 mV and an efficiency of 17.0% of a cell using the simplified selective emitter process. The bulk lifetime of Cz-Si was monitored during a selective emitter process with a screen printed aluminium BSF on the rear. The bulk lifetime of the as grown wafer was 32 µs and was subsequently improved by phosphorous gettering to 67 µs. Bulk lifetime was further raised to 120 µs through aluminum gettering of the screen printed BSF. This result has to be taken into account when applying alternative rear sides with dielectric passivation where beneficial aluminium gettering cannot be used. Therefore material that does not strongly depend on aluminum gettering should be used. A dielectric rear side passivation can be integrated at several stages in the production process. Each sequence entails different challenges especially in maintaining the rear side passivation quality at the end of the process.
Keywords: Selective Emitter, Czochralski, Gettering

1 INTRODUCTION

One of the paramount objectives of today`s solar cell research is the reduction of the cost per watt peak. This can either be achieved by reducing the production cost of the cells or by increasing the cell efficiency with only a moderate raise of the cell production cost. Cell concepts like the buried contact cell of BP Solar [1], the HIT cell of Sanyo [2] or the IBC cell by Sunpower [3] are concepts that generally achieve very high efficiencies. These cell concepts suffer on the other hand by increased production costs.

Currently, the standard cell process of applying screen printed front side contacts on top of a PECVD SiN layer and a full area aluminum BSF on the rear side clearly dominates the market.

This work focuses on the improvement of the cell production process using screen printed emitter contacts on the front. The goal is to assess the improvement in cell efficiency that can be achieved by applying a selective emitter design and a dielectrically passivated rear side.

Several concepts have been proposed for the formation of a selective emitter structure [4, 5, 6]. Although lab experiments have shown them to perform better than its homogeneous counterpart the selective emitter design has so far not been applied in an industrial production when screen printing is used for emitter metallization.

We show emitter saturation measurements that give a quantitative assessment of the front side emitter quality including different passivation layers. Furthermore, we present monitoring results of the bulk lifetime of standard p-doped Cz-wafers using an extended screen printing / buried contact process. Finally, several process sequences to apply a dielectric rear side passivation are discussed with regard to possible obstacles and requirements to the introduction of the specific dielectric layers.

2 SELECTIVE EMITTER CONCEPTS

A conventional homogeneous emitter has to fulfill two conflicting boundary conditions: it should be lowly doped to limit the recombination losses and secondly, doping must be high enough to reach an acceptable low contact resistance of the front grid metallization.

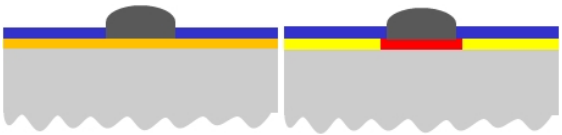

Figure 1: Homogeneous (left) and selective (right) emitter.

The sheet resistance is a characteristic value of the doped emitter and is limited in the standard screen print process to about 50 Ω/□. One way to improve solar cell efficiency is to optimize the emitter, Ag-paste and firing conditions. Another possibility is to change the front side into a selective emitter structure. The selective emitter structure decouples the above mentioned boundary conditions. A schematic of a selective emitter structure is shown in Fig. 1 (right). It features a highly doped region underneath the metallized contact region and a lowly doped area in the emitter between the front grid. The highly doped regions can be easily contacted by the Ag-paste during the firing step in a belt furnace. The emitter regions between the contact grid can be lowly doped to reduce recombination losses. A selective emitter structure can be realized in several process sequences and the emitter quality can be quantitatively characterized by the emitter saturation current (j_{0e}).

2.1 Design of experiment

The emitter saturation current was measured on symmetrical samples. FZ wafers were used to reduce the influence of bulk lifetime in the results and wafers (crystal orientation was <100>) were polish etched by CP6 solution. A reference sample was prepared by a double- sided $POCl_3$ diffusion with an industrial type 50 Ω/□ emitter. Both sides were also SiN coated by low frequency direct plasma PECVD. This sample was fired in a belt furnace to reproduce the front side of an industrial screen printed solar cell.

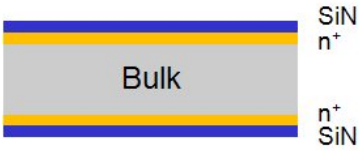

Figure 2: Symmetrical sample for j_{0e} measurement.

The emitter saturation current – including the surface passivation as applied in a solar cell – was measured by Quasi Steady State Photo Conductance (QSSPC). Measurements were performed in high injection conditions.

The reference sample with the homogeneous 50 Ω/□ emitter and PECVD SiN has a j_{0e} of about 400 fA/cm^2 before the firing step and 220 fA/cm^2 after firing. The behavior of reducing j_{0e} after firing is well known [7].

The contribution of the front side to the saturation current of a solar cell consists of the emitter saturation current and the saturation current of the metallised region j_{0eM}. The latter is in general higher than j_{0e} due to the increased recombination at the metal contacts. In case of a selective emitter design higher doping underneath the metal contacts may reduce recombination due to a more effective front surface field. On the other hand it increases recombination in the doped region. In the following section two process schemes are presented to realize a selective emitter structure. The emitter saturation current was measured on samples representing only the emitter area without the contact region.

2.2 Selective emitters with two diffusion steps

A selective emitter can be realized by two diffusion steps including a patterned mask. The heavily diffused regions can be realized as shown in Fig. 3 (left side, named process a)). The wafer must be covered with a diffusion barrier layer, e.g. SiN or thick SiO_2. The layer is then selectively opened by a laser. A subsequent heavy diffusion occurs only in the laser opened area. In this case a 10 Ω/□ diffusion was used. The thickness of the SiN layer is reduced during the heavy diffusion by about 30 nm, the remaining SiN is removed by hydrofluoric acid (10%). A light diffusion (100 Ω/□) creates a high efficiency emitter. A SiN layer for surface passivation must be applied and the remaining process steps are similar to a standard screen printing process (printing and drying front and rear side & firing). Due to the order of diffusion there is no influence of the heavy diffusion on the emitter. This process requires in addition to the two diffusions also two SiN deposition steps. Symmetrical samples for j_{0e} characterization are realized by the light diffusion and the SiN passivation (both sides) and firing.

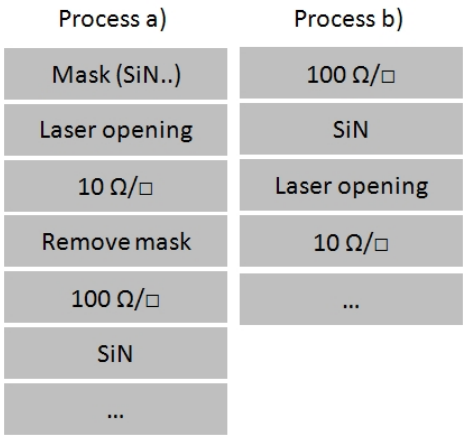

Figure 3: Process schemes with two diffusion steps

Another possibility for the formation of a selective emitter structure with the use of only one SiN deposition is shown in Fig. 3 (right side, named process b)). Beginning with the light emitter diffusion, deposition of SiN follows. The SiN layer is again structured by a laser. A heavy diffusion is applied in the areas where the SiN has been removed by laser ablation. The SiN layer thickness must be chosen adequately to have the proper thickness at the end of the process. The contact regions are not covered by SiN in this process. This process sequence is utilized in the buried contact cell process, the sequence to form the front side is the same as shown here. The opened heavy diffused area can be plated by nickel and copper. Besides the buried contact process, this sequence is also used by the "semiconductor finger" concept [6]. The symmetrical samples for j_{0e} determination were realized as shown in Fig. 3, process b) including the heavy diffusion, except for the selective opening of the SiN layer by the laser.

The results of the j_{0e} measurements are shown in the table below.

Table I: Emitter saturation current densities

	Reference 50 Ω/□ PECVD SiN	Process a) PECVD SiN	Process a) SiO_2+ PECVD SiN	Process b) PECVD SiN	Process b) LPCVD SiN
J_{0e} (fA/cm^2)	220	90	40	140	120

The emitter saturation current was reduced to 90 fA/cm^2 using process a) with a 100 Ω/□ emitter. This value can be further reduced to 40 fA/cm^2 when applying a 20 nm thick thermal SiO_2 layer after the light diffusion. J_{0e} values obtained by process b) structures are higher, 140 fA/cm^2 using PECVD SiN and 120 fA/cm^2 respectively by using LPCVD SiN. LPCVD SiN is normally used in buried contact processes to avoid pinholes even on untextured surfaces that would lead to overplating during metallization.

To explain the J_{0e} values shown in table I, three different effects have to be considered. At first, a drive-in step was applied in process b) during the heavy diffusion, thus changing the emitter profile. Secondly, during the heavy diffusion step effusion of hydrogen from SiN occurs [8]. In addition, the surface passivation quality of the SiN layer is likely to be affected by the heavy diffusion. For j_{0e} all these effects may play a role.

2.3 Selective emitters with one diffusion step

Only one diffusion step can be sufficient to form a selective emitter structure when using a diffusion suppressing, laser structured mask. The process sequence is shown in Fig. 4.

Figure 4: Single diffusion selective emitter process

The process starts by applying a thin mask. The mask can be made of SiN, SiO_2 or porous silicon. The thin layer is then selectively opened by a laser. In the laser opened regions the heavy diffusion leads to a low sheet resistance, whereas the remaining area (covered by a thin mask) has a higher sheet resistance. The thin mask serves only as a diffusion suppressing layer. The remaining process steps after the heavy diffusion are the same as in a standard screen print process.

Porous silicon can be fabricated by wet chemical etching in a $HF/HNO_3/H_2O$ solution. Layer thickness can be optically controlled since porous silicon has a lower refractive index and interference effects lead to a colored layer. A challenging issue is the damage-free removal of porous silicon by a laser in the front grid area. Chemical laser damage etching is not possible since it would also etch the porous silicon in the emitter region between the fingers. Experiments have shown that the treatment (cleaning steps and drying) between the porous silicon formation and heavy diffusion is critical and can lead to a strong variation of the sheet resistance after the diffusion.

SiN can be deposited with a homogeneous thickness on large areas and is chemically resistant to alkaline chemical etching. Thus the laser damage after structuring the thin layer of SiN can be removed. For this investigation SiN was chosen to optimize the process on cell level. SiN thickness and diffusion parameters have to be adjusted to reach the desired sheet resistances in the highly as well as the lowly doped regions. A SiN thickness of 30 nm in combination with a 20 Ω/□ diffusion led to the desired 100 Ω/□ sheet resistance in the emitter region. Nevertheless, this process is also critical to small process parameter variations.

2.5 Cell results

Reference cells using a standard screen printing process and homogeneous 50 Ω/□ emitter were manufactured on boron doped Cz-Si wafers. Process a) and simplified process c) was used to process selective emitter solar cells. Sheet resistance in the heavily doped region was 10 Ω/□ in process a) and 20 Ω/□ in process c), sheet resistance in the emitter region were 100 Ω/□ for both selective emitter processes. All cells have a full area aluminum BSF. Cell area was 25 cm^2, bulk resistance 1.5 Ωcm, and no texture was applied. The IV-data of the best cells are shown in table II.

Table II: IV-data of selective emitter solar cells compared to a reference cell with homogeneous 50 Ω/□ emitter. The improvement is 10 mV in V_{OC}.

Best Cell	FF (%)	J_{SC} (mA/cm²)	V_{OC} (mV)	η (%)
Hom. emitter (50 Ω/□)	76.7	33.8	625	16.2
Process a) 2 diffusions	77	34.6	635	16.9
Process c) 1 diffusion	78.1	34.4	635	17.0

The best solar cell of the reference process has an open circuit voltage of 625 mV, the best cells of both selective emitter processes have open circuit voltages of 635 mV. The 10 mV increase in V_{OC} shows the improvement on the front side due to the selective emitter structure. The short circuit current was also improved by 0.6 mA/cm^2 in process c) and 0.8 mA/cm^2 in process a) respectively. Maximum efficiency was raised from 16.2% to 17.0% (untextured cells). The increase in current is due to a better blue response as shown in the IQE below.

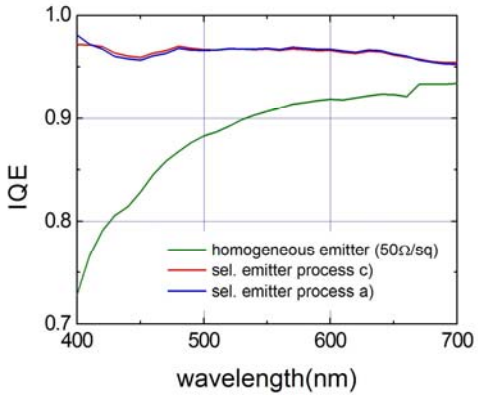

Figure 5: IQE of the best solar cells in the short wavelength region. The increase in short circuit current density of the selective emitter cells is due to a better blue resonse.

2.6 New selective emitter approach (one diffusion)

A new selective emitter process is developed that uses only one diffusion step. The sheet resistance deviation on test samples was found to be only +/- 5 Ω/□ on a 100 Ω/□ emitter. Emitter saturation current density was measured on emitters created by the new approach. Surface passivation was done by a double sided PECVD SiN deposition and firing in a belt furnace. The j_{0e} measurement results of this emitter depending on the sheet resistance are shown in table III. One has to notice that j_{0e} was already lowered when the sheet resistance was the same as in the reference sample (50 Ω/□). This new approach is patent pending [9].

Table III: J_{0e} values of the emitter created with the new approach. Even with the same sheet resistance of 50 Ω/□ as for the reference sample, j_{0e} is lowered to 160 fA/cm^2.

	Reference 50 Ω/□ PECVD SiN	New process 50 Ω/□	New process 100 Ω/□	New Process 150 Ω/□
J_{0e} (fA/cm^2)	220	160	80	90

3 BULK LIFETIME MONITORING OF CZ-SI DURING SOLAR CELL PROCESS

The optimization of the front side of solar cells was discussed in sections above. The bulk silicon material should exhibit high lifetimes in order to achieve good spectral quantum efficiency for long wavelength photons. It is well known that the bulk lifetime can change during the solar cell process. There is the possibility of phosphorous and aluminum gettering to improve the bulk-lifetime during the process and hydrogenation can passivate recombination centers. This is often important for mc-Si to passivate e.g. grain boundaries and seems to be less important for monocrystalline silicon. Nevertheless, the bulk lifetime of Cz-Si was monitored during a selective emitter process including the screen printed aluminum BSF formation.

3.1 Design of experiment

Neighboring Cz-Si wafers with a bulk resistance of about 1.5 Ωcm were chosen and process b) described in section 2.2 was applied. Starting with a light diffusion, the single sided LPCVD was followed by a heavy diffusion. The final process step was screen printing aluminum on the rear side and firing in a belt furnace. This process represents also the essential process steps of the buried contact process used at the University of Konstanz. After each process step one wafer was taken from the sample batch. After the process was completed, the SiN layer as well as the aluminum BSF and the emitter were removed by wet chemical etching. The surfaces were passivated with an Iodine/Ethanol solution and the lifetime was measured by microwave photo conductance decay (µPCD).

3.2 Results: bulk lifetime monitoring during process

The lifetime of the as grown material was 32 µs as can be seen in Fig. 6. It was improved to 49 µs due to phosphorous gettering during the 100 Ω/□ diffusion. The single side LPCVD SiN deposition further improves lifetime to 55 µs. The LPCVD SiN deposition is carried out at a peak temperature between 750°C and 800°C with the 100 Ω/□ emitter still present on both wafer sides, and therefore gettering continues. The following heavy diffusion is done at 950°C and bulk lifetime was raised 67 µs. The largest improvement could be realized by screen printing aluminum on the rear side and firing. Final bulk lifetime was 120 µs.

The investigated Cz grown silicon showed a strong dependence on aluminum gettering. The exact material properties e.g. carbon and oxygen concentration leading to this behavior must be further investigated. It is important to consider the bulk lifetime especially when a dielectric rear side passivation is to be used instead of the Al BSF – with the absence of aluminum gettering the minority carrier lifetime may in some instances suffer.

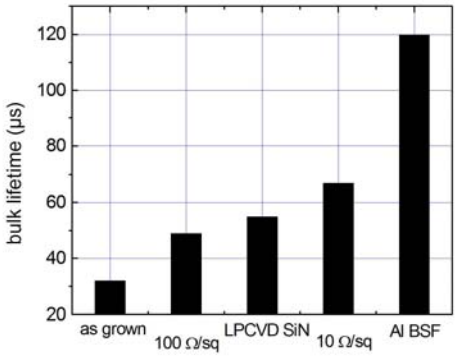

Figure 6: Bulk lifetime monitoring during process b) including aluminium BSF formation. Subsequent improvement during process with a big raise through aluminium gettering.

4 DIELECTRIC PASSIVATION OF THE REAR SIDE

Most industrially produced solar cells feature a full area aluminum BSF generated by screen printing and sintering of aluminum containing paste. This technology entails several drawbacks: 1. The difference of aluminum and silicon with regard to their thermal expansion coefficient leads to wafer warping during the sintering process [10]. Excessive warpage makes the cells unsuitable for module interconnection. The recent decrease of the wafer thickness, a trend that is widely expected to continue, has aggravated these warpage difficulties. 2. Especially for thin solar cells the reflective properties of the rear side become crucial for the cell performance as their impact on light trapping increases. The mediocre reflectivity of a screen printed aluminum BSF is expected to further limit the quantum efficiency for long wavelength photons. 3. Although applying a strong field effect passivation of the rear side, the BSF has shown to be inferior to several dielectric passivation layers with respect to its surface recombination velocity.

A passivating dielectric layer for the rear side can be integrated at several stages of the production process. Three examples are given below.

Table IV: Examples for different stages at which a dielectric passivation on the rear of the cell can be applied.

Dielectric Rear Passivation	Emitter diffusion/ARC	Emitter diffusion/ARC
Emitter diffusion/ARC	Dielectric Rear Passivation	Front Contact Formation
Front Contact Formation	Front Contact Formation	Dielectric Rear Passivation
Rear Contact Formation	Rear Contact Formation	Rear Contact Formation

Each of the examples given in the table above entails different challenges.

In the example on the left the dielectric passivation is applied prior to the diffusion step. This means that the layer has to maintain its passivating properties

throughout several production steps with high thermal load (diffusion, sintering of front contacts). Furthermore it has to be resistant to the chemical baths applied after the diffusion.

The processing scheme shown in the center in table IV features the dielectric passivation after the diffusion process. Thus the thermal load is strongly reduced and limited to the metallization process.

In the third processing scheme shown on the right in table IV the dielectric passivation is applied after the sintering of the front contacts. In this case surface cleaning of the rear side without attacking the metal finger grid on the front side and / or contamination of the deposition device by the metallization on the front seems to be the most difficult task.

Four different passivation layers have so far been successfully applied for rear side passivation: SiO_2, SiN, SiC and amorphous silicon. The use of SiO_2 as a passivation layer in the processing scheme described on the left in table IV carries several challenges. The emitter diffusion and HF-cleaning attack the silica. Thus the SiO_2 has to be grown very thick which in turn increases the thermal load on the wafer. SiO_2 can also be grown after the diffusion passivating both the emitter and the base substrate. Since SiO_2 grows much faster on highly doped substrates the emitter will be covered by a much thicker layer of SiO_2 than the undoped rear side. In order not to adversely affect the antireflection properties of the cell the silica would have to be removed from the emitter side of the cell along with the highly doped layer that has been oxidized. This makes contacting by screen printing more difficult.

SiN, SiC and amorphous silicon can in principle be applied in all processes that are shown in table IV. While the passivating properties of amorphous silicon are known to suffer from a high thermal load resulting from the emitter diffusion and contact firing, both SiN and SiC may yet prove to be suitable to be introduced into the production process at an earlier stage.

4 SUMMARY

Possible improvements to the widely used standard screen printing process were investigated. Several processes to change the front side to a selective emitter structure were presented, including emitter saturation current measurements on symmetrical samples. The reference sample with an industrial homogeneous 50 Ω/□ emitter and fired PECVD SiN has a j_{0e} of 220 fA/cm^2. On selective emitter structures with two diffusion steps, using first a 100 Ω/□ diffusion then a SiN layer as mask and finally a 10 Ω/□ diffusion, j_{0e} is 140 fA/cm^2 using PECVD SiN and 120 fA/cm^2 respectively with LPCVD SiN. By changing the sequence of light and heavy diffusion and applying PECVD SiN for surface passivation, j_{0e} was measured to 90 fA/cm^2. Solar cells were made with a two step selective emitter and a simplified process with a single diffusion step using laser structured SiN as diffusion suppressing layer and no texture was applied to these cells. The best reference cell with homogeneous 50 Ω/□ emitter has an efficiency of 16.2% and 625 mV V_{OC}. The best selective emitter solar cells with both used processes have a 10 mV increase of V_{OC} leading to 635 mV and an efficiency of 17.0% of a cell using the simplified selective emitter process. A disadvantage of the simplified process with the diffusion suppressing layer is the difficult reproducibility since small process variations can lead to strong varying results. To overcome this problem a new selective emitter process was presented, featuring only one diffusion step. Sheet resistance homogeneity was very good and j_{0e} was measured to 80 fA/cm^2 using low frequency direct plasma for surface passivation. Additionally, the bulk lifetime of Cz-Si was monitored during a selective emitter process with a screen printed aluminium BSF on the rear. The bulk lifetime of the as grown wafer was 32 µs and was subsequently improved by phosphorous gettering to 67 µs. Bulk lifetime was further raised to 120 µs through aluminum gettering of the screen printed BSF. This result has to be taken into account when applying alternative rear sides with dielectric passivation where beneficial aluminium gettering cannot be used. Therefore material that does not strongly depend on aluminum gettering should be used. A dielectric rear side passivation can be integrated at several stages in the production process. Each sequence entails different challenges especially in maintaining the rear side passivation quality at the end of the process. Laboratory solar cells achieved good results with dielectric rear side passivations (Laser Fired Contacts by Fraunhofer ISE or iPERC by IMEC). The combination of an improved emitter combined a high efficiency rear side scheme is still challenging, especially by realizing the structure cost effective by using screen printing metallization, few additional process steps and Cz grown silicon.

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