CRYSTALLINE Si THIN FILM n-TYPE SOLAR CELLS: A SCREEN PRINTED REAR JUNCTION APPROACH

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ABSTRACT: In this work we present large area crystalline silicon thin film n-type solar cells. The rear junction is formed by growth of an n-type Chemical Vapour Deposition (CVD) layer on highly p^+-doped substrate.The arising rear side emitter geometry of the solar cell features an n^+ phosphorous diffused front-surface-field on n-type thin absorber deposited by high temperature CVD. Apart from the deposition of the thin film all processing steps rely on already industrially implemented processing steps such as open tube furnace $POCl_3$ diffusion, PECVD SiN_x deposition and thick film screen printing technique. Following simulations, different base doping levels of the CVD layers were tested. The best 96 cm^2 large solar cell with a 30 µm thick epitaxial wafer equivalent showed an efficiency of 13.5% for a p^+ Cz-Si substrate and 12.3% for the best mc-Si device, respectively.
Keywords: thin film crystalline silicon, n-type solar cell, rear junction

1 INTRODUCTION

The feedstock shortage of the last years led to various efforts to either save material or at least to harness sources that so far had no relevance for solar cell processing because of their high doping level or doping polarity. Thus cell concepts on crystalline n-type substrates occurred [1,2] with promising results for rear emitter devices [2,3,4]. Thereby the emitter was formed in general by a recrystallised Al-doped rear eutectic deriving from an Al paste firing step. Simulations based on first experimental results for multicrystalline n-type rear junction Si solar cells predicted a good cell performance of this kind of solar cell even for a wafer

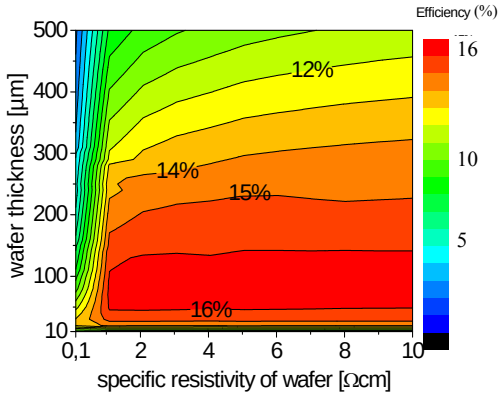

Figure 1: Contour plot from PC1D simulations for n-type rear emitter solar cells showing the cell efficiency as a function of wafer thickness and base doping [2]

thickness below 50 µm as can be seen in Figure 1. Of course, so far handling and manufacturing of such thin devices is too delicate. But crystalline Si thin film technology has the potential to replicate the cell geometry by creating a thin n-doped silicon layer on a conductive substrate. In our case the deposited so called wafer equivalent, representing the bulk material of our solar cell, was grown on a highly doped Si base substrate. The stack of wafer equivalent and base substrate can be handled in the following just like a standard silicon wafer and enables a simple transfer to an industrial production.

In this work we demonstrate a thin film approach to the rear emitter n-type cell concept using an n-doped epitaxial CVD-Si layer grown on a highly p-doped Si substrate being both, substrate and emitter of the solar cell. We show a large area near-production process on Cz and mc substrates and discuss the results.

2 EXPERIMENTAL

2.1 CVD Si layer

The CVD layers were deposited at IMS-Chips in a lamp heated barrel reactor (Applied Materials). In order to remove any contamination a Piranha cleaning of the chemical polished substrates took place before the deposition. To avoid effusion of dopants from the substrate during the high temperature epitaxial depositon the highly doped Cz substrates were covered with a Low Temperature Oxide (LTO) on the rear side of the device. To avoid any contamination of the processing chamber by the multicrystalline metallurgical grade backing material a 50 Ω/sq pre-gettering $POCl_3$-diffusion with subsequent removal of the top 10 µm of the wafer was performed. At a temperature of 1100°C the epitaxial layers were grown at atmospheric pressure under hydrogen atmosphere using trichlorosilane (TCS) as gaseous precursor. In a turbulent gasflow ambient and with a growth rate of 0.8 µm/min the deposition took place in the quartz bell jar. For the doping of the wafer equivalent phosphine was added to the processing gas.

2.2 Sample processing

Highly boron-doped Cz p-type Si wafers with a resistivity in the range of 14-19 mΩcm served as substrate as well as refined metallurgical grade multicrystalline Si wafers of the same doping level. The mc neighboring substrates were cut from an ingot grown at Elkem. The carrier concentration of all base substrates

is approximately one order below the boron concentration known from p-type boron emitters [5]. However, due to the thickness of the base substrate of 240-700 µm the substrates have a sheet resistance of 0.3-1 Ω/sq and are perfectly suited as an emitter if combined with an n-type layer. The epitaxial n-type film was deposited with a thickness of 30 µm at three different doping concentrations. By varying the phosphine gas flow for three different chemical vapour depositions bulk resistivities of 0.8, 4 and 30 Ωcm were established on the pre-cleaned and polished wafer surface. As a result of the different doping polarity of substrate (p^+) and CVD layer (n), the pn rear junction of the device is already formed during the deposition of the epitaxial Si-film.

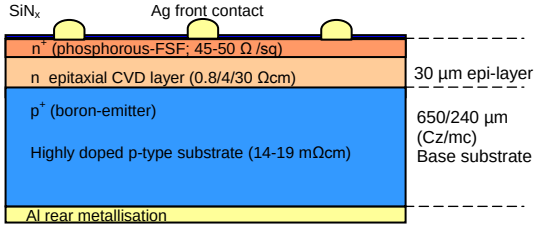

Figure 2: Sketched cross section of the thin film solar cell

The process sequence continues with a front side KOH+IPA (isopropanol) texture for the Cz substrate and alkaline etching for the mc devices, respectively. The following tube furnace $POCl_3$-diffusion forms the front surface field with a sheet resistance of 50 Ω/sq and qualifies the device for suitable contacting by silver

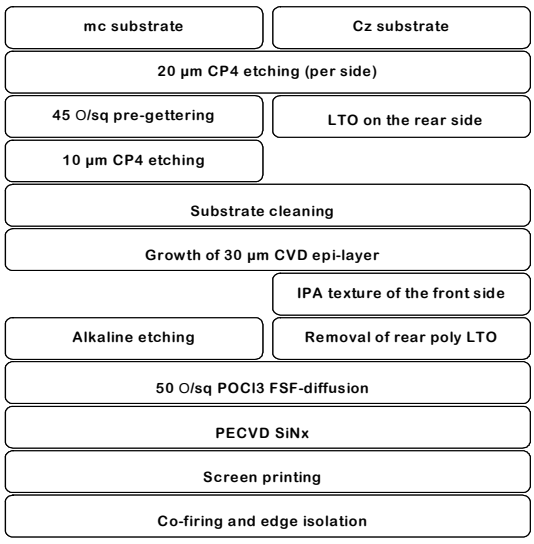

Figure 3: Flowchart of the solar cell processes on Cz as well as on mc-Si CVD epi-layer printed on the sample

thick film metallisation. Subsequently the deposition of 75 nm PECVD SiN_x represents the antireflection and front side passivation of our thin film solar cell. In a next step the silver finger grid at the front side and a closed Al rear electrode are screen printed. The cell process is finished by co-firing of the metal contacts in a belt furnace and edge isolation by a dicing saw. Cz and mc substrates differed significantly in thickness ($\Delta d \sim 500$ µm) and in addition revealed diverse surface morphologies. Despite these facts, no adjustment of the firing conditions was necessary. The assumed reasons will be discussed in the next section.

Figure 3 graphically summarizes the basic processing steps for the device sketched in Figure 2.

3 RESULTS AND DISCUSSION

3.1 Best solar cells

In our investigations the epitaxial layers deposited at IMS-Chips Stuttgart were manufactured in a simple industrial process as described above. For our best solar cell, an efficiency of 13.5% was obtained on 96 cm^2, with an open circuit voltage of 622 mV, indicating the good performance of the solar cell structure. Table I summarizes the parameters of the best solar cells on Cz and mc-Si. The substrate thickness of 650 µm for monocrystalline devices faced a nearly three times thinner mc-Si base material.

Table I: Parameters of the best solar cells on Cz and mc-Si substrates with an area of 96 cm^2

	Resist. [Ωcm]	**FF** [%]	**V_{OC}** [mV]	**J_{SC}** [mA/cm^2]	**η** [%]
Cz	4	79	622	27.4	13.5
mc	0.8	78.3	613	25.6	12.3

Despite of that difference the metal contact formation of both types took place at nearly the same temperature profile in the belt furnace and resulted in excellent fill factors for either solar cells. This high firing tolerance of the process can be explained by the rear emitter geometry. Shunting of the device at the n^+n front side is almost impossible and therefore opens space for a wide variation of firing parameters.

3.2 Rear junction

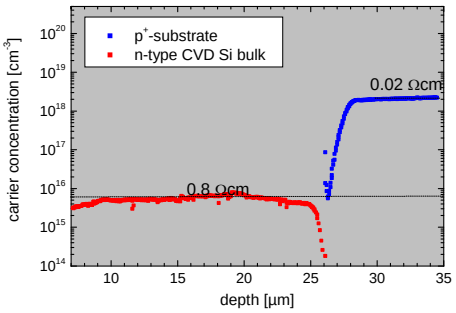

Figure 4: Carrier concentration profile of the n-type absorber and rear np^+ junction measured by ECV profiling technique

The carrier concentration of a monocrystalline 0.8 Ωcm device was measured by Electrochemical Capacitance-Voltage (ECV) profiling technique. Of special interest was carrier concentration close to the intersection of substrate and thin film layer. The p^+n transition ranges about 3 µm. The flat slope at this interface may result from a diffusion of carriers out of the highly doped substrate into the epitaxial layer during the high temperature vapour deposition. Below and above that region follow stable and flat plateaus. The carrier concentration of $7x10^{15}$ cm^{-3} for the n-type CVD Si bulk

is in good accordance with the resistance identified by a four point probe measurement. The same can be attested for the p^+ substrate with a corresponding value of $3x10^{18}$ cm^{-3}.

3.3 Solar cells with different base doping

Three solar cell batches with different doping levels were performed on Cz and mc-Si substrates. Table II shows the averaged parameters of each group representing in general 4 to 5 devices.

Table II: Solar cell parameters of processed mc and Cz Si solar cells. The data represents averaged values of the batches

Si	Res. [Ωcm]	FF [%]	V_{OC} [mV]	J_{SC} [mA/cm^2]	H [%]
mc1	0.8	77.6	611.7	25.6	12.1
mc2	4.0	75.9	608.8	26.2	12.2
mc3	30	74.9	606.3	26.0	11.8
Cz1	0.8	78.0	622.4	26.2	12.7
Cz2	4.0	79.1	621.0	27.1	13.3
Cz3	30	77.45	617.2	27.3	13.1

Several information can be extracted from the table: the highest average efficiency is found for group Cz2 with a doping level of 4 Ωcm including the best monocrystalline solar cell. The lower doped devices follow but are clearly superior to the samples of group Cz1 with the highest doping concentration of the wafer equivalents. As could be expected, increasing bulk resistivity leads to a drop in V_{oc} for mc-Si as well as for Cz thin film solar cells. On the other hand the short current densities J_{sc} behave the other way round and

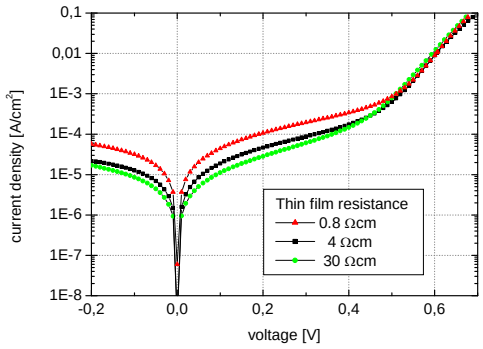

Figure 5: Dark IV curve for cells with different doping levels of the epi-layer

enhance with increasing bulk resistivity at least for the monocrystalline devices. For the mc-Si solar cells the current optimum was found for the group of medium doped layers. Considering the thickness of the active layer of less than 30 µm and the fact, that n-type silicon features high lifetimes and small capture cross sections of recombination-active defects, the effective lifetimes should not be the limiting factor of the device. Finally it can be stated, that in general all parameters of the mc-Si solar cells are inferior in direct comparison to Cz values.

It should be noted that all these values just show a tendency as for a real statistic the number of processed wafers was too small.

Figure 5 shows the dark IV data for three Cz samples of the different resistivity batches. They just differ in their shunt resistances which are all at a high level of 2-$5x10^5$ Ωcm^2.

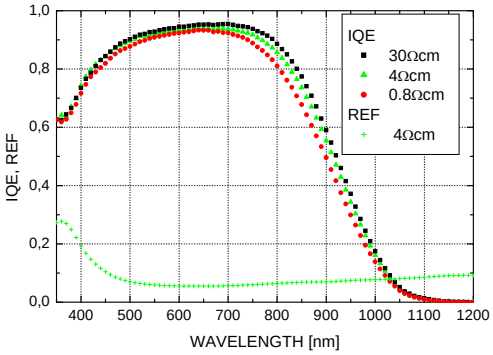

Figure 6: IQE and reflectance of textured solar cells on Cz-Si substrate

The Internal Quantum Efficiency (IQE) of the monocrystalline solar cells show a quite regular behaviour in the mid-range wavelengths of the light spectrum which is comparable to what can be detected for standard crystalline Si solar cells. In contrast a dramatic decline in quantum efficiency occurs at the borders of the considered spectrum. The drop for the blue response is owed to the simple front side passivation scheme. The thickness of the active wafer of just 25 µm switches significantly the ratio of bulk volume to surface compared to a standard wafer. As a consequence the surface affects more strongly the characteristic of the device. For future work a selective front-surface-field would be a way to pay more attention on that issue [6]. On the other side the average penetration of long wavelength photons is deeper than the epitaxial grown layer and these photons are therefore lost for the carrier generation. Intermediate reflective films [7] are a good possibility to recover these losses. The increasing current densities for lowly doped wafer equivalents correspond to a better spectral response especially in the long wavelength region and might indicate higher effective minority carrier lifetimes for these CVD layers. Another explanation indeed is more likely and regards a variation in thickness for the different batches of wafer equivalents. Front side etching took the same time for all devices but Si with higher carrier concentration is removed more easily. For that reason the weaker doped wafer equivalents might have a thicker absorber layer with a better red response.

4 SIMULATION AND OUTLOOK

Figure 7 shows the results of a PC1D simulation on the basis of first experimental cell results on Cz-Si substrates. Especially two main facts are to be pointed out: there is in general good accordance with the measured data for changed thickness and resistivity. However, the drop in efficiency while changing the epi-layer´s resistivity from 4 to 30 Ωcm could not be found in the simulated data. An explanation might be a

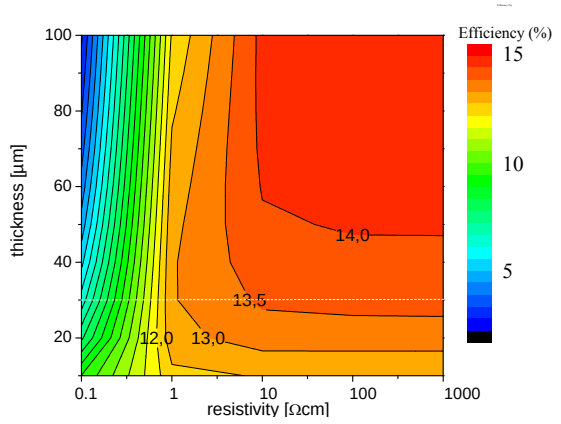

Figure 7: Simulated efficiencies according to thickness and resistivity of CVD wafer equivalent

deformed shape of the doping profile at the junction and therefore a changed space charge region for lower doped wafer equivalents. Although the illustrated parameters in the simulation do not admit much more space for further enhancement, increased power output is still possible for a slightly changed design of the solar cells. Improved front side passivation or selective front surface field adjustment as well as a rear reflector on thinned substrates are supposable. This would lead to a solar cell performance with more than 15% efficiency.

5 CONCLUSION

We have shown a simple thin film approach of an n-type Si solar cell with a rear side emitter. Thereby the substrate of the wafer equivalent builds at the same time the emitter of the device. Apart from the chemical vapour deposition of the epitaxial layer all further steps fall back on processes that are already implemented in PV industry. The used n^+np^+ geometry has resulted in large area (96 cm^2) solar cells with an efficiency of 13.5% for epi-layers on highly doped Cz Si substrate and 12.3% for a mc-Si base material. Simulations revealed the potential for further improvement of the structure and show that devices with more than 15% are feasible with our simple process.

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