QUANTITATIVE COMPARISON OF DIFFERENT GEOMETRIES FOR HIGHVO SOLAR CELLS

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ABSTRACT: In the theoretical description of monolithically integrated HighVo solar cells their characteristic feature – deep insulation trenches and remaining wafer bridges between the unit cells – have to be considered. The bridges cause leakage currents which we describe by an additional shunt resistance R_p. Different geometries for these wafer bridges lead to different equivalent circuit models for the corresponding HighVo solar cells. In this paper we compare two geometries. The "standard" geometry, using one insulation trench per unit cell and the "frame" geometry defined by one meander shaped insulation trench per HighVo solar cell. For both cases the basic device behavior is discussed and for one special case quantitatively compared. The frame geometry exhibits higher conversion efficiencies (approx. 1% absolute) at low illumination intensities although the unit cells are driven at different operating points.
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1. INTRODUCTION

Over the last three years new concepts for monolithically integrated non-thin-film crystalline silicon solar cells have been developed at the University of Konstanz [1-4]. The main purpose of these so called high voltage ("HighVo") solar cells is to provide a charging unit for applications where voltages of several volts are desired and a light exposable area of more than approximately 10 cm^2 is available. Advantages compared to conventional series connected solar cells are the cost reduction with respect to the manual tabbing of many small size solar cells and a very aesthetic optical appearance.

A characteristic feature of HighVo solar cells are trenches reaching from the wafer front surface to the back surface which enable the partial insulation of unit cells (UCs) as well as their series interconnection [1]. In the theoretical description of the HighVo solar cells the remaining wafer bridges between the UCs - which hold the device together - have to be considered. The emitter-free, non-carrier collecting wafer bridges cause leakage currents and a lowered over all shunt resistance $R_{sh,eff}$. Different geometries for these wafer bridges lead to different equivalent circuit models for the corresponding HighVo solar cells as will be shown further below.

It is obvious that the area, number and structure (front or back contacted) of the UCs of a HighVo solar cell always have to be optimized for a certain application (e.g. off grid security surveillance, mobile phones etc.). For example, in mobile consumer articles it is necessary to supply a sufficiently high voltage for loading accumulators already at indoor light intensities and spectral distributions. With standard crystalline silicon solar cells as well as HighVo solar cells this is hard to achieve. As the low intensity performance of a c-Si Solar cell is dominated by its shunt resistance the major challenge in optimizing HighVo solar cells for these applications is to increase the resistance of the wafer bridges.

In this paper we concentrate on the discussion of $R_{sh,eff}$ obtained by two different geometries for the wafer bridges; changes by using wafer material of a higher resistivity ρ are not in the scope of this work. The geometries to be compared are the "standard" geometry, which is the most basic geometry as already described in [1-4], and the "frame" geometry mentioned in [3,4]. Please note that these wafer bridge geometries are independent of the UC design (e.g. front or back contact UCs).
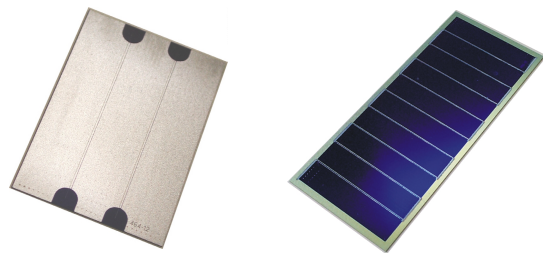

Figure 1: Photographs of fabricated HighVo solar cells using an emitter wrap through design for the unit cells. Left: standard geometry, without ARC; Right: frame geometry, with ARC.

2. THE STANDARD GEOMETRY

HighVo solar cells in the "standard" geometry (SG) have an insulation trench and two remaining wafer bridges between neighboring UCs. The resistance of the bridges is controlled by 1) the length of the insulation cut in the wafer (i.e. how much of the bridge remains), 2) the area around the bridges where the emitter and back contact are avoided in order to decrease conductance (see Fig 1, left) and 3) the resistivity of the wafer material. A photograph of an emitter wrap through (EWT) [5] type HighVo solar cell in the SG is given in Fig. 1 (left); a schematic drawing of one of the bridges is given in Fig. 2. Applying the standard two diode model for a UC and allowing for the conductivity of the two wafer bridges by a resistor R_p the resulting equivalent circuit [6,1] for four UCs is shown in Fig. 6 (left). All UCs, except the one which carries the emitter contact to form the output of the device – called UC1 – are additionally shunted by R_p. If series resistance R_s is negligible the total effect of R_{sh} and R_p can be approximated by a single resistor $R_{sh,eff} \approx R_{sh}R_p/(R_{sh}+R_p)$ in parallel to the diodes.

The basic features of the HighVo solar cells arising from this model are summarized by Fig. 3, which shows the calculated dependence of η and V_{mpp} on the number of

UCs M for several illumination intensities F and two different scenarios (simulation input parameters see Fig. 3):
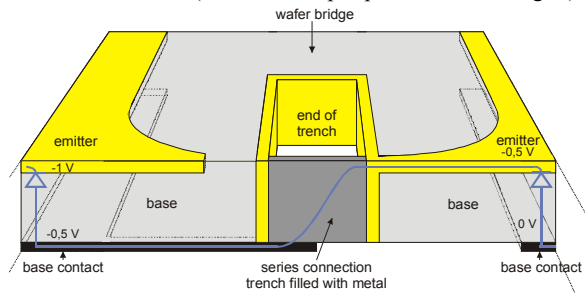

Figure 2: Wafer bridge, insulating trench, metal series connection and voltage conditions close to V_{oc} between two UCs. The shorted emitter region at the left wall and the end of the insulation trench is a residual one due to the applied process sequences [2,4]. Using a 10 Ωcm material, a bridge width of 2 mm and an emitter free area of 0,4 cm² an R_p of approximately 300 Ω is obtained (two bridges per UC !).

A) The UCs have a fixed area. With every additional UC the area of the HighVo solar cell increases.

With increasing M the efficiency decreases until at about M = 10 a constant value is approached. The decrease is due to adding more and more R_p-shunted UCs to UC1. For M < 10 the positive influence of UC1 – which is not shunted by R_p – is still detectable. For M > 10 the benefit of the higher effective shunt of UC1 becomes negligible; the performance of the HighVo cell and that of a normal series connection of solar cells without R_p ($R_{sh,eff}$ being their R_{sh}) are equivalent. Please note that these conclusions depend on the values used for R_p, the area of the UCs and R_{sh}.

B) The HighVo solar cell has a fixed area. With every additional UC the UCs have a reduced area. The absolute value of R_p remains constant because of the geometry of the wafer bridges.

With decreasing UC area shunting by R_p gets more and more severe. Therefore increasing M means also decreasing $R_{sh,eff}$ and the HighVo cell performance suffers with every added UC. There exists no limiting value for η for large M like in scenario A). At low F some voltages can not be reached even by adding up an infinite number of infinitesimal small UCs.

In the calculations the additional loss in active cell area by the increasing number of wafer bridges in the HighVo cell has been neglected to highlight the influence of R_p only. Including this effect η decreases more rapidly for all F. The case of an area loss of 0,2 cm² per UC and its consequences at F = 5 mW/cm² is indicated by the crosses in Fig. 3.

Fig. 4 shows the computed dependence of η and FF on F and R_p for a 98 cm² HighVo solar cell consisting of 14 UCs using the equivalent circuit for the SG. Because the area loss for increasing R_p depends on several parameters and is ambiguous it has been neglected again. Compared to reference calculations obtained from an ideal series connection of 14 solar cells without R_p but using $R_{sh,eff}$ as R_{sh} (not shown) the results for $R_{sh,eff}$ > 150 Ωcm² and F > 1 mW/cm² are – as expected – almost identical. One major difference occurs at lower $R_{sh,eff}$ where the FF can increase again. This effect is due to UC1. At low $R_{sh,eff}$ the other UCs are completely shunted and represent merely a resistor contacting UC1. The FF of UC1 dominates then the FF of

the whole HighVo solar cell, although this higher FF is not correlated with a higher conversion efficiency of the device.
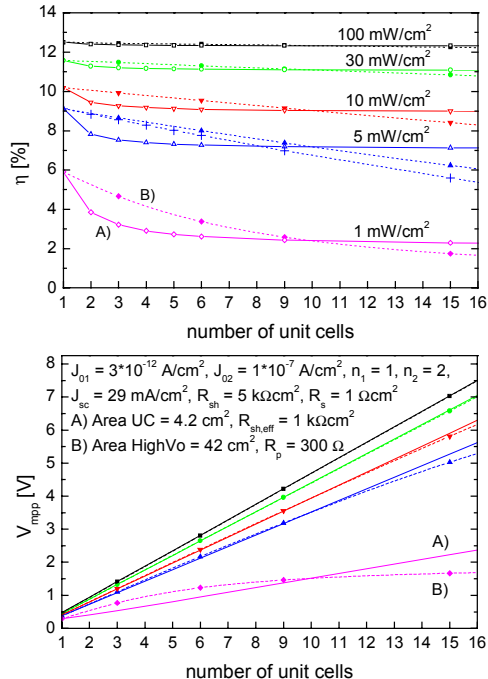

Figure 3: Calculated dependence of η and V_{mpp} on the number of UCs for two different scenarios. A) The UCs have a fixed area. With every additional UC the area of the HighVo solar cell increases. B) The HighVo solar cell has a fixed area. With every additional UC the UCs have a reduced area. The simulations have been performed for several F; simulation input parameters are given in the inset. An R_{sh} typical for large scale produced screen printed solar cells was assumed.

Ideally R_p should be of the order of 10^6 Ω with only R_{sh} limiting $R_{sh,eff}$. Within the HighVo concept this will not be achievable. A prerequisite for a reasonable low intensity performance compared to conventional screen printed Si solar cells should be $R_p \approx R_{sh}$, allowing $R_{sh,eff}$ > 1 kΩcm². When realizing wafer bridges as described in Fig. 2 and using material with a specific resistance of 10 Ωcm an R_p of 300 Ω is obtained. For UC areas larger than approx. 3,5 cm² this R_p enables an $R_{sh,eff}$ > 1 kΩcm² depending on R_{sh}.
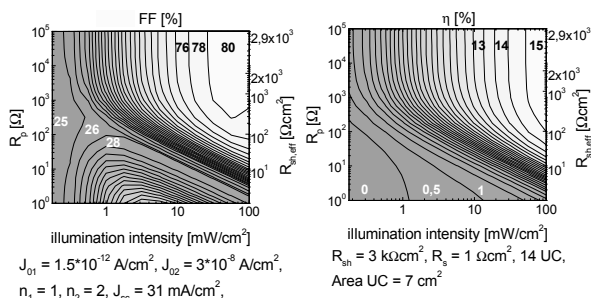

Figure 4: Calculated dependence of η and FF on F and R_p for a 98 cm² HighVo solar cell consisting of 14 UCs. In contrast to single solar cells the FF exhibits a drop and following increase with decreasing F or R_p while η does not.

3.   THE FRAME GEOMETRY

The "frame" geometry (FG) follows the idea of creating longer high resistive wafer parts connecting the UCs without losing too much active cell area. This is realized by introducing a meander shaped insulation trench leading to a non-carrier collecting frame of wafer material (see Fig. 5). The distance between UCs across the bridges of the frame is given by the width of the UCs themselves improving the resistance of the connecting parts compared to the standard geometry. Using a UC width of 7 mm, a frame width of 2 mm, $\rho = 10$ Ωcm an $R_p = 1440$ Ω (together with a reduced loss in effective area) can be expected from a two dimensional calculation.
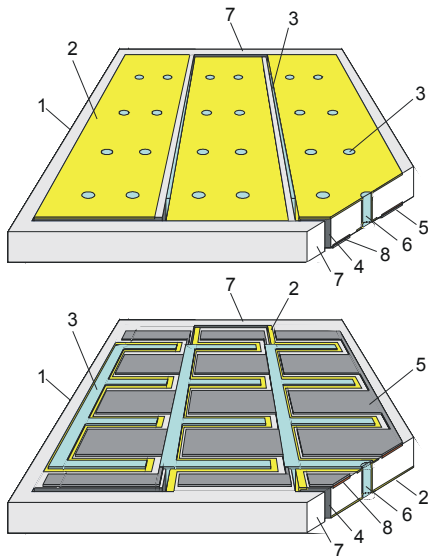

Figure 5: Front (upper) and backside view (lower drawing) of an EWT type HighVo solar cell in the frame geometry. 1: wafer, 2: emitter, 3: emitter contact, 4: insulation trench, 5: base contact, 6: hole, 7: wafer bridge, 8: BSF. Series connection is obtained by filling the insulation trenches with conductive material.

The meander shaped insulation trench leads to a different equivalent circuit model [4] (Fig. 6, right) as only second next UCs are connected by the wafer bridges whereas the electrical series connection exists between neighboring UCs. Fig. 7 illustrates the definition of the resistors used in the equivalent circuit.

The achievable performance improvement at low illumination intensities from the FG is not immediately obvious. E.g. the diodes of UC3 are now bypassed by three resistors, R_{sh} and two $R_{p,i}$. Not only $R_{p,i}$ is increased but also the voltage across these resistors and the parasitic currents which doubled. Making the very imprecise assumption that UC3 is in effect shunted by R_{sh} and twice by $R_{p,i}/2$ – and using the data from Fig. 9 – an $R_{sh,eff}$ of 1200 Ωcm^2 is obtained. For a HighVo solar cell in the SG with the same active area a $R_{sh,eff} = 940$ Ωcm^2 is calculated, indicating that the FG might offer some efficiency gain at low intensities. But still the wafer bridges will have a dominant influence on the effective shunt resistance of the device.

In order to elucidate the conditions in the FG where the performance of the single UCs are not as independent of

each other as in the SG we calculated the "effective" IV characteristics of the UCs. While ramping the voltage at the outputs of the HighVo solar cell and monitoring the corresponding current also the voltage across the diodes and R_s of each UC was monitored. From these voltages and the corresponding current of the HighVo cell the effective IV characteristics of the UCs during operation of the whole device are obtained. This procedure reduces the FG equivalent circuit to an ordinary series connection of non-identical UCs which in total reproduce the behavior of the device [4]. The effective IV characteristics can be fitted by the two diode model to determine effective shunt resistances of the UCs which result from the interplay of the various parts of the HighVo solar cell. We such obtain quantifiable parameters. Fig. 8 shows the potential drop at the UCs and the resulting IV-characteristics which exhibit an imbalance in the HighVo cell. The fitted $R_{sh,eff}$ for UC1 to UC10 are 3000, 1300, 820, 960, 910, 960, 820 and 1300. With UC6 as a center of symmetry opposing UCs show a similar behavior.
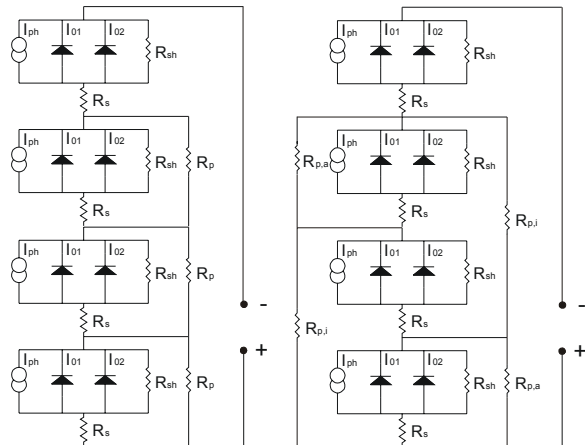

Figure 6: Equivalent circuit models for the SG (left) and FG (right) in the case of 4 UC. In each case the UC at the top of the drawing represents UC1.
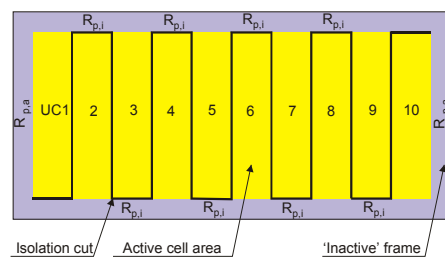

Figure 7: Schematic drawing of the FG for 10 UC. Second next UCs are connected by wafer bridges defining $R_{p,i}$. The wafer frame around UC1 and UC10 defines two resistors $R_{p,a}$. Note that the pn-junction of UC1, through which the current leaves the device is not shunted via $R_{p,a}$ because $R_{p,a}$ only connects the base of UC1 (see Fig. 6).

Although the diodes and the R_s of the different UCs have been chosen to be identical Fig. 8 shows that the UCs are not current matched exactly and mismatch losses are introduced by the FG. These losses can be reduced by adjusting the areas of the UCs similar to the procedure in [1] but presumably will not lead to dramatic improvements.
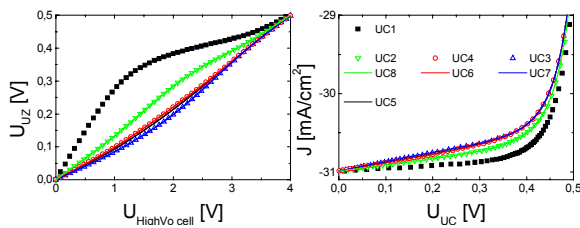
Figure 8: Potential drop across the diodes and Rs for the different UCs and the resulting "effective" IV-characteristics of the UCs in the HighVo solar cell.

The calculated low intensity performances of two HighVo solar cells in the SG and FG with identical size and effective area are shown in Fig. 9. As expected from the above arguments there is an improvement in efficiency and voltage for intensities below 20mW/cm^2. The maximal gain in η is approx. 1.1 % absolute (19% relative) at $F \approx 3$ mW/cm^2; V_{mpp} increases by about 460 mV at $F = 1$ mW/cm^2. From further calculations it can be concluded that the over all low intensity performance of the above HighVo solar cell in the FG is comparable to conventional series connected identical UCs with an R_{sh} of approx. 1300 Ωcm^2.

Additionally shown is the performance of an equivalent HighVo cell in the SG with reduced R_p and therefore increased active cell area. A corresponding wafer bridge design was used in [7].

4. REVIEW OF EXPERIMENTAL RESULTS

In an experimental study EWT type HighVo cells in the FG with a larger width of the UCs (9.2 mm) but same UC area as above exhibited an over all effective shunt resistance of approx. 2000 Ωcm^2, which is comparable to standard screen printed Si solar cells [3]. This result is also due to a very good R_{sh} of more than 10kΩcm^2. Using our standard process, the 10 Ωcm high resistivity CZ wafers exhibit a deeper pn-junction and little defects thereby reducing ordinary shunting mechanisms compared to screen printed mc Si solar cells.

Because R_p defined by the bridges does not scale with the UC area (the parasitic currents through the bridges will stay the same independent of UC size) any increase in the area allows major improvements in the low intensity performance of the FG as well as the SG. With a UC area of 5.2 cm^2 and somewhat larger emitter-free areas an $R_{sh,eff}$ of 1800 Ωcm^2 has also been achieved with EWT-HighVo cells in the SG [4].

$R_{sh,eff}$ depends critically on the length of the insulation trench which clearly has an impact on the mechanical stability of the device. Good stability during processing is achieved by cutting the trenches only as long as necessary for the metal series connection. Once the trenches have been filled with metal the devices are less fragile and the trenches can be enlarged by laser cutting afterwards. Because the bridges are emitter free there is no damage introduced into the pn-junction of the UC. In the FG the meander shaped trench is completed in a similar two step procedure [4]. An approach using a supporting substrate and separating the UCs completely has been described in [3]. Obviously further improvement in $R_{sh,eff}$ is possible by using material of a higher resistivity although the output voltage at high illumination intensities will be reduced.

The highest conversion efficiency obtained with HighVo solar cells so far is 12.8 % (6 UC, $V_{oc} = 3.5$ V) [3].
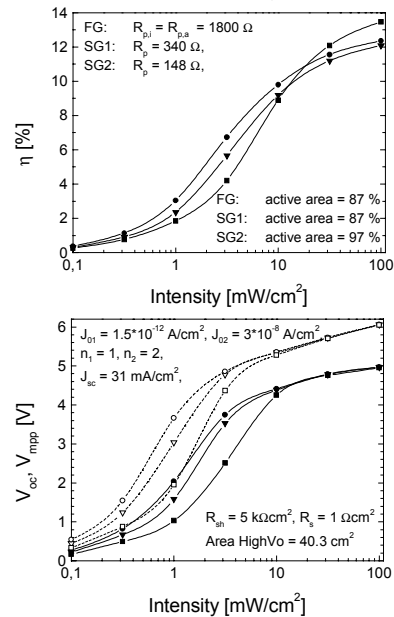

Figure 9: Low intensity performance of two HighVo solar cells – each consisting of 10 UCs – in the SG and FG with identical size and active area. Additionally shown is the performance of a equivalent HighVo cell with reduced R_p and therefore increased active cell area (SG2).

5 CONCLUSION

The consequences of two different geometries (standard and frame geometry) for fabricating HighVo solar cells have been discussed. A general result of the imperfect insulation of the UCs is that a certain UC area (with our approach approx. 3.5 cm^2) and a certain loss in active area (approx. > 0.3 cm^2 per UC for FG) are necessary to achieve an $R_{sh,eff} > 1$ kΩcm^2. Although the resistance of the wafer bridges in the FG itself is much higher than in the SG (here approx. factor of 4) the resulting improvement in efficiency at low illumination intensities is – in the investigated example - restricted to at most 1.1% absolute. This is due to the consequences of the wafer frame apparent from the equivalent circuit. Additionally the UCs in the frame geometry are driven at different operating points leading to mismatch losses. Experimentally an $R_{sh,eff}$ of approx. 2000 Ohm cm^2 has been achieved with the FG (UC area 3.9 cm^2). Higher $R_{sh,eff}$ seem only possible with larger UC areas or wafer of higher resistivity.

REFERENCES
[1] S.Keller et al., J. Appl. Phys., **87** (2000) 1556
[2] S.Scheibenstock et al., Sol. En. Mat. Sol. Cel. **65** (1-4) PVSEC11- Part I (2001) 179.
[3] Keller et al., Proceedings 16th EC PVSEC (2000) 1218
[4] Keller, Thesis, University of Konstanz (2000)
[5] Gee et al., Proceedings 23rd IEEE PVSC (1993) 265
[6] Valco et al., Proceedings 15th IEEE PVSC (1981) 187
[7] Neu et al., this conference