LOW COST P^+NN^+-TYPE BACK JUNCTION SOLAR CELLS BY SCREEN PRINTING TECHNIQUE ON CZ AND MC-SI MATERIAL

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ABSTRACT: We present p^+nn^+ back junction solar cells on n-type silicon (Si)-material processed with a low cost screen printing technique. The p^+n-junction is formed by a uniform layer of aluminium (Al) screen printed on the rear side resulting in a device with back junction geometry. On a Czochralski (Cz)-Si substrate, a solar cell efficiency of 15.3% was obtained. The device featured excellent open circuit voltage V_{oc}= 623 mV (FF= 77.9%, J_{sc}= 31.4 mA/cm^2, A= 4 cm^2, W= 230 µm). A comparably high V_{oc} of 616 mV for a multi-crystalline (mc)-Si solar cell confirms the high quality of the used material and led to a cell efficiency of 12.9% (FF= 76.6%, J_{sc}= 27.3 mA/cm^2, A= 4 cm^2, W= 230 µm). Optimisation of emitter homogeneity on large areas resulted in a fill factor of FF= 81% on mc-Si substrates. Simulations based on the measured solar cell parameters showed a potential for cell efficiencies close to 16%.
Keywords: n-type, multi-crystalline Si, back junction

1 INTRODUCTION

The PV sector enjoys since years a boom reflected in continuous double-digit rates of growth and Si is responsible for over 90% of the market. It is conceivable that the available feedstock of the so far dominating p-type Si alone will no longer satisfy the demand and it is unavoidable to open up new resources. There is a reject of n-type Si material from the electronic industry in the same abundance as for p-type (>2000 t/a) [1]. For this reason, n-type Si may become an important base material for solar cells in the near future to guarantee further unhindered growth.

In addition, n-type Si in comparison to p-type Si has a lack of recombination centres in the bulk such as boron-complexes (B-Fe, B-O, etc.) possibly leading to higher and more stable effective lifetimes of the minority charge carriers [2]. Therefore, effective diffusion lengths in n-type Si are expected to be higher, thus opening up the alternative of rear junction solar cells even on mc-Si substrates.

Recently, a few solar cell concepts on various n-type Si materials have been presented as an alternative to the state of the art p-type technology. Among these, solar cells with back junction geometry have shown interesting and promising results. The back junction concept has been applied to dendritic web [3], Czochralski (Cz) and multi-crystalline (mc) Si material [4] as well as on Float Zone (FZ) Si wafers [5]. The solar cell processes applied so far for the back junction concept include low cost belt furnace sequences [3] or high efficiency steps such as photolithography, double antireflection coating [4] or even back contact cell geometry [5] for FZ Si material.

In this work, we present solar cell development on n-type Cz and mc-Si material applying the back junction concept with low cost processes for industrial use. Attractive features compared to the alternative of a front (boron diffused) emitter are, for example, processing steps, avoiding a higher thermal budget and therefore possible thermal degradation of the mc-Si material. In addition, a lower series resistance of the assembly (front Ag instead of Al metallisation) can be achieved with a single print. Another reason that argues for the proposed approach is the exclusive use of established industrial manufacturing steps, which offers an immediate integration of n-type solar cell processing.

The main requirement of the back side concept is the need for high quality material. The characterisation showed very high minority charge carrier lifetimes for as-grown Cz-Si (440 µs) as well as for mc-Si after gettering (220 µs) averaged over the entire wafer. The diffusion lengths corresponding to such high lifetimes make the application of the back junction concept attractive when the substrate thickness is less than 200 µm. A detailed characterisation of the mc-Si wafers with a focus on lifetime measurements [6] and another approach using an industrial cell process on this n-type material applying B-diffusion for a front junction device [7] can be found in additional papers published at this conference.

2 EXPERIMENTAL PROCEDURE

Except for the first step, the applied rear junction process sequence is based on the industry standard n^+pp^+ process shown in Figure 1. It starts with wafer thinning to about 230 µm followed by saw damage removal. The thinning was done either by wet chemical CP4 etching or later by mechanical abrasion as the starting substrate thickness exceeded 300 µm. In an industrial process, this step would not be necessary when wafers are cut to a thickness of 230 µm or less.

In the next process step, only if thinning has been done by abrasion, the surface damage is removed by an NaOH etch followed by industrial cleaning. Then a front surface field (FSF) with a sheet resistance of 45 Ω/sq is formed by $POCl_3$ diffusion. After the deposition of a PECVD SiN_x layer, serving as surface passivation and antireflection coating, metal pastes are screen printed on the rear (closed Al contact) and on the front (Ag finger contacts) and co-fired in a belt furnace. For optimisation purposes in some cases an intermediate step in the

standard process consisting of Al printing, firing and etching was introduced. In order to achieve a homogeneous and closed Al-emitter after co-firing of the pastes, a detailed examination of cleaning conditions, the use of different Al-pastes and the optimisation of firing parameters have been performed and evaluated. Finally, p^+n-junction isolation using a dicing saw was performed.

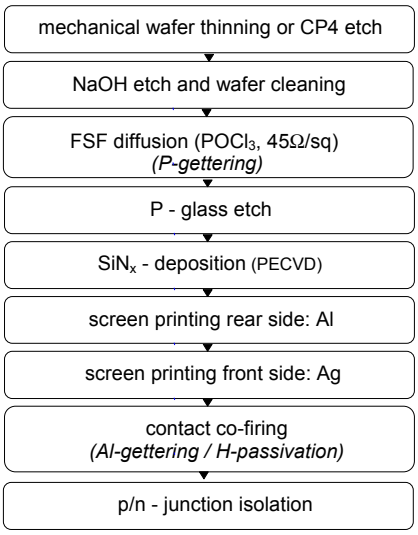

Figure 1: Basic process sequence of our standard back junction solar cell.

The applied process already includes P- and Al-gettering as well as H-passivation steps, leading to effective lifetimes of the minority charge carriers of >220 µs averaged over the entire mc-Si wafer [6].

3 RESULTS AND DISCUSSION

3.1 Al-emitter optimisation

Different Al pastes were tested to achieve the most homogeneous p^+-region.

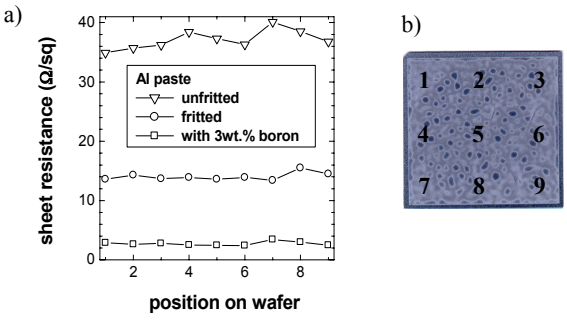

Figure 2: a) Sheet resistance depending on paste and position on the Si-wafer (25 cm^2). **b**) Picture defining the different positions.

For identical firing conditions, the sheet resistance is very dependent on the paste used, and varied between 35 and 2.5 Ω/sq. The uniformity of the sheet resistance measured on each 25 cm^2 Cz-Si wafer as depicted in Figure 2 was good.

Solar cells processed with the standard process (Fig. 1) using standard firing conditions, pastes, etc., suffered from a poor fill factor (FF) as a consequence of a low shunt resistance R_{shunt}. In order to improve the FF of the back junction solar cell concept, several modifications of the standard process were tested. In a first step, the alloying temperature of the aluminium was changed from standard p-type solar cell conditions (process A) to parameters that guaranteed a homogeneous Al-emitter formation (process B). As firing through the phosphorous doped region with the Ag-fingers is not a problem, higher temperatures were applied. In general, best results were obtained with fast firing at high temperatures and the use of an unfritted Al-paste. For further optimisation, the processing of the Al doped p^+-region and of the backside metallisation was separated. Therefore, an intermediate step of Al printing, firing and etching was introduced after the deposition of the SiN_x layer (process C). Both changes improved the FF of the solar cells significantly, as can be seen in Figure 3a). This improvement is due to an increase in R_{shunt}, which was extracted from the dark IV-characteristics (Figure 3b)) using the 2-diode model.

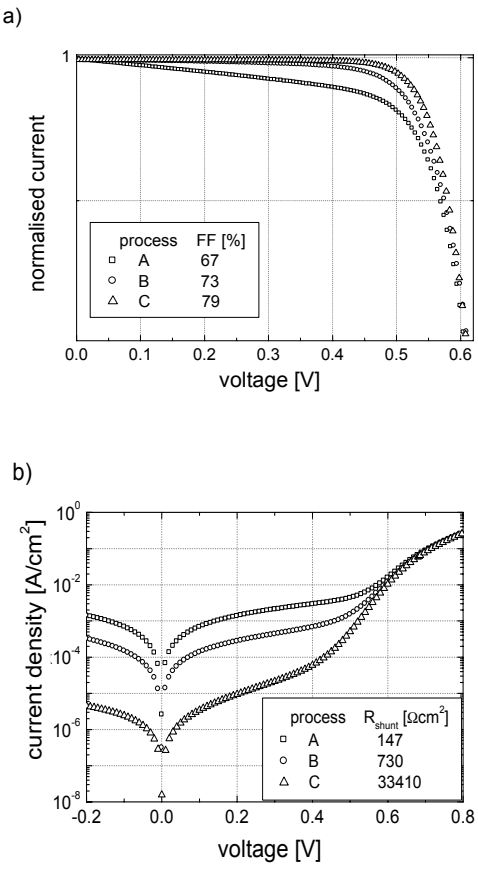

Figure 3: a) Illuminated and **b)** dark IV-characteristics for different processing sequences A, B and C.

Results on solar cells fabricated with process C are summarised in section 3.2.

3.2 Parameters of best solar cells

With this low cost approach, high open circuit voltages of up to 625 mV on Cz-Si substrates (5 Ωcm) and 616 mV

on mc-Si substrates (1.7 Ωcm) were achieved, proving the excellent quality of both materials and good properties of the surface passivation.

Based on the theorem of Swanson and calculations of Cuevas [4], assuming typical values for the recombination current density in an Al alloy p^+ region, 641 mV present the theoretical limit for the achievable open circuit voltage. Our results are close to that limit (623 mV) and demonstrate the potential of n-type Si material for industrial use. High fill factors of up to 79% were obtained on Cz-material. Table I summarises the solar cell parameters for the best Cz-Si and mc-Si back junction solar cell produced with processing sequence C.

Table I: Parameters of rear junction solar cells processed on n-type Cz and mc-Si (A= 4cm^2, W= 230 µm).

material	ɛsistivity [Ωcm]	FF [%]	J_{sc} nA/cm^2	V_{oc} [mV]	η [%]
Cz-Si	5	77.9	31.4	623	15.3
mc-Si	1.7	76.6	27.3	616	12.9

Both solar cells have an excellent V_{oc} but a rather moderate J_{sc}, thus further improvement of the cell concept will focus on increasing J_{sc}.

An excellent fill factor of 81% has been achieved recently with process B on large area substrates and confirms the high quality of the Al-paste based emitter.

3.3 Edge isolation

Some features of our back junction device are quite different to conventional p-type solar cells. For example, applying our processes, it was necessary to cut through the aluminium alloy to obtain sufficient edge isolation. Otherwise, due to the double-sided $POCl_3$ diffusion, there is a disturbing p^+n^+ transit on the rear side. This tunnelling diode causes shunts at the edges of the cell.

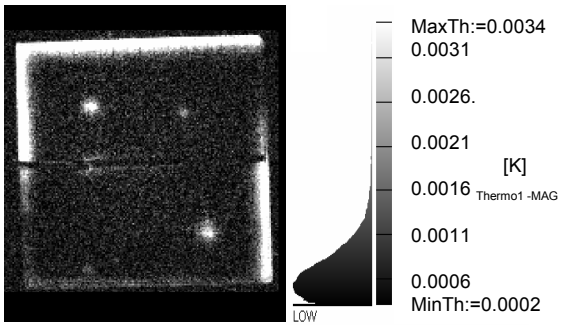

Figure 4: IR-thermography after insufficient edge isolation. Especially the top edge is completely shunted because of a p^+n^+ short circuit transition.

Figure 4 shows a thermographic picture of such a cell with the edge isolation used for standard p-type cells. The cell suffers from huge edge shunting problems visible as a light stripe especially at the top edge. There are several possibilities to avoid this problem. Either, nearly the whole surface must be Al printed or the P-diffusion step must be processed just single sided (e.g. spin-on / spray-on process, screen printing) or the n^+-layer must be removed from one side in an additional step before the screen printing procedure. The last possibility has been successfully tested demonstrating the applicability of our process to large area solar cells.

3.4 Simulation of back junction devices

The experimental investigations were compared with PC1D simulations paying special attention to the influence of wafer thickness and bulk resistivity on the solar cell efficiency. Experimentally extracted parameters from e.g. IV, lifetime and ECV measurements served as a starting point for the variation of the material properties. Figure 5 illustrates modelled efficiency as a function of specific resistivity and substrate thickness.

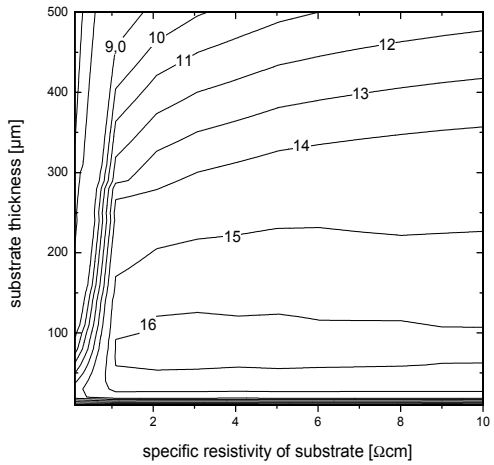

Figure 5: Efficiency dependence on substrate thickness and specific resistivity.

The results shown in Figure 5 demonstrate that the efficiency on substrates with specific resistivity below 1.5 Ωcm is limited to about 11%. To reach efficiencies above 15%, a substrate resistivity higher than 2 Ωcm and wafer thickness below 230 µm is necessary. 16% efficiency marks an upper limit for this simple process, because reaching higher efficiencies would require a wafer thickness below 180 µm which is too delicate to process with the present processes. With the implementation of advanced processes (selective FSF, buried contacts, etc.), this limit must be recalculated and a further increase of the efficiency above 17% is expected.

4 CONCLUSIONS AND OUTLOOK

This paper summarises our work on p^+nn^+ back junction solar cells on n-type Si- material with low cost processes. Although the process was accomplished by screen printing technique, excellent open circuit voltages of V_{oc} = 623 mV and fill factors of up to FF = 77.9% were achieved. The best results were 15.3% efficiency on Cz-Si and 12.9% for a mc-Si solar cell. Newest results have shown that the intermediate etching step described in process C is not necessary to obtain good cell

performances as attested by a large area solar cell with a FF of 81% on a mc-Si substrate. Therefore, ongoing experiments on larger areas with both Cz-Si and mc-Si solar cells look very promising.

PC1D simulations show that by thinning the substrate to 180 µm, efficiencies of nearly 16% are feasible with this low-cost method. Higher efficiencies (>17%) are expected with further optimisation of the individual process sequences such as the ARC and the emitter formation as well as with the implementation of advanced processing sequences (selective FSF, buried contacts, etc.).

The main challenge is a further improvement of the short circuit current. So far J_{sc}= 31.4 mA/cm^2 for Cz Si and J_{sc}= 27.3 mA/cm^2 for mc-Si have been realised. Future efforts will therefore focus on the increase of the efficiency by e.g. the use of thinner substrates. In addition, we plan to resign the $POCl_3$–diffusion for the front surface field to obtain a better yield for short wavelengths, increasing the spectral response of high energy photons. To avoid high series resistance of the front metallization, buried contacts in heavy diffused grooves will be applied. As the surface recombination velocity of SiN_x-passivated surfaces is rapidly decreasing with lower doping [8] an additional increase in V_{oc} is expected.

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