14.4 % Screen Printed n-Type mc-Si Solar Cells with Al Back Junction on Thin Large Area Wafers

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Abstract: This paper presents back junction n-type Si solar cells on large area mc-Si wafers processed with low cost techniques. Due to a pn junction formed by screen printed Al paste the process is exclusively based on already established and familiar techniques known from standard p-type material processing. This low cost approach resulted in a solar cell efficiency of up to 14.4% for a 151 cm^2 multicrystalline n-type Si wafer.

Key Words: n-Type mc-Si, Si Solar Cells, Al-Emitter

1 Introduction

The development in the PV market is at present very dynamic. This enjoyable fact holds also challenges. Among those the occurring silicon shortage must be seen as a main problem. The situation suggests breaking new ground such as using n-type silicon as substrate. There are several reasonable points why to concentrate on that material: it has been shown, that it is less sensitive to metallic impurities [1] and for some cleaning techniques it seems to be advantageous in terms of MG silicon purification.
A precondition to avail these advantages is the development of an industrial procedure competitive to the state of the art p-type solar cell processing.
In this paper we attend to one possible approach and present a low cost solar cell process by screen printing metallisation on n-type multicrystalline Si substrates. The solar cells are processed in back junction geometry with a screen printed contact and Al-emitter.

2 Experimental results

2.1 Material Characterisation

Besides multiple n-type ingots grown with different resistivitiy ranges and different doping elements [2], an additional experimental ingot was solidified at Deutsche Solar. The silicon substrates used in our experiments originated from this directionally solidified experimental ingot. The material features an extraordinary trend of the bulk resistivity: at first from bottom to top the specific resistivity increases from 60 to values of around 1000 Ωcm at wafer number 125 and then decreases to 1 Ωcm at the very top position as shown in Figure 1. Seebeck measurements confirm a switch of the ingot doping from p-type at the bottom to n-type at positions above 125. Chemical analysis by GD-MS at Fraunhofer ISE confirmed that the ingot is doped with both Sb and B as impurities, whose increasing concentration at different rates along the ingot explain the shape of the curve in Figure 1. In a first experiment wafers evenly spread over a whole column were manufactured with the same in 2.2 described solar cell process distinguished by the fact that it is working as well on p-type as on n-type silicon base material.

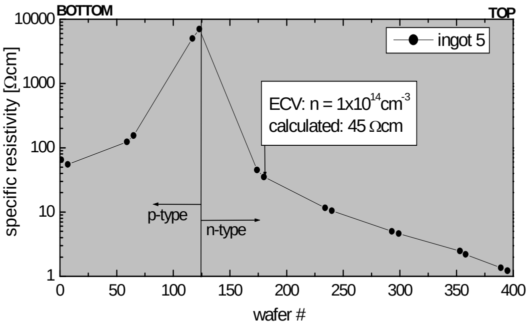

Figure 1: Specific resistivity of the wafers according to the position in the ingot measured by four point probe. Around wafer number 125 the doping changes from p- to n-type.

2.2 Solar Cell Process

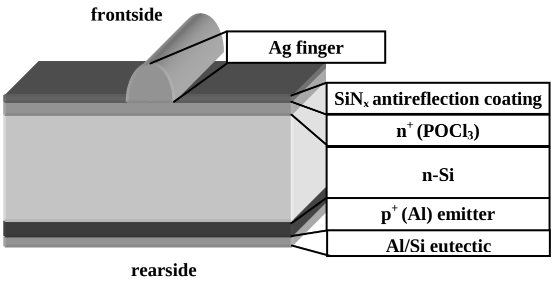

Figure 2: Formal structure of the FSF solar cell on n-type substrate.

As the n-type base cells featured back junction geometry, the 270 µm thick as-cut wafers had to be thinned to 200 µm which was done in our case by a CP4 etching step. The following sequence was applied, based on the industry standard n$^+$pp$^+$ process sequence optimised for Al back junction processing.

The process starts with NaOH etching and industrial chemical cleaning (HCl, HF) followed by the formation of a n^+ layer on the front side with a sheet resistance of 45 Ω/sq by $POCl_3$ diffusion, serving as a Front Surface Field (FSF) for the n-type substrate or as an emitter for the p-type substrate. After the deposition of a PECVD SiN_x layer on the front side, serving as surface passivation and antireflection coating, the rear phosphorous diffused layer is removed by another alkaline etching step. Afterwards the metal pastes are screen printed on the back (closed Al contact) and on the front (Ag finger contacts) and co-fired in a belt furnace. The Al forms the emitter for the n-type substrate. In the case of the n-type substrate, we call this the FSF cell concept that is also known in literature as the Phostop concept [3].

2.3 Cell Results

The processing showed remarkable results (Fig. 3). Particularly two things were eye-catching: the constant increase of the efficiency from top to bottom without a drop or dip at the changeover from p-type to n-type and the good results for n-type cells with a specific resistivity in the range of 10 to 100 Ωcm. In lifetime mappings with µW-PCD on passivated as-grown wafers in this resistivity range two different regions were visible as depicted in Figure 4 a). The average lifetime measured over the entire wafer area was 280 µs. Wafers from this resistivity region were used for further process optimization because of the suitable properties for the FSF-concept. After optimisation of the process, concerning mainly the firing conditions, efficiencies of up to 14.4% on a 151 cm^2 were reached (cell parameters in Table 1).

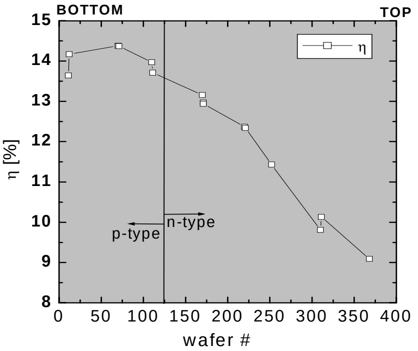

Figure 3: Efficiency of solar cells depending on the wafer position in the ingot. All solar cells were processed in the same way.

	area [cm^2]	**res.** [Ωcm]	**FF** [%]	**J_{sc}** [mA/cm^2]	**V_{oc}** [mV]	**η** [%]
mc-Si	151	~50	76.6	31.7	604	**14.4**
mc-Si	25	~50	72	33.4	608	**14.8**

Table I Parameters of best solar cells obtained by the process

Figure 4 b) shows a light beam induced current map taken at 980 nm representing the internal quantum efficiency of the best large area n-type mc solar cell. As can be seen from this Figure the inhomogeneities in lifetime of the as-grown material were nearly homogenised by the cell process. Nevertheless a 25cm^2 solar cell cut from the centre of this cell led to a current density of 33.4 mA/cm^2 and a cell efficiency of 14.8%. Investigations are on the way to improve the fill factors.

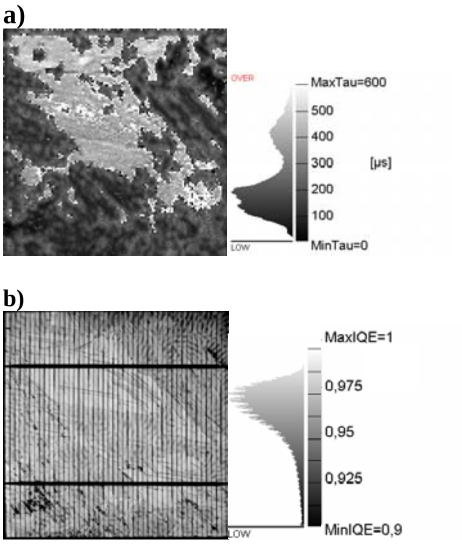

Figure 4: a) Lifetime mapping on as-grown wafer with µW-PCD and SiN_x passivated surface.
b) LBIC map of the so far best large area n-type mc solar cell taken at a laser wavelength of 980 nm.

Earlier results of Al back junction cells with FF> 78% [4] agree with solving this problem very quickly. Further improvement as e.g. using isotextured substrates makes efficiencies exceeding 15% feasible. At the same time the transfer and optimization of the process to mc-Si material with lower bulk resistivity is on the way.

3 Conclusions and Outlook

We have presented a low cost solar cell process for n-type mc-Si wafers which has resulted in an efficiency of 14.4% for a cell area of 151 cm^2. With the improvement of the cell concept, efficiencies around 15% are feasible. The exclusive use of already established and familiar industrial techniques make this process very attractive for industrial applications. The possibility of short time introduction of this cell concept into the PV market could be a way to open up the idle n-type feedstock material relieving the current shortage of Si sources.

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