APCVD BASED STACKED CO-DIFFUSION FOR MULTICRYSTALLINE SILICON P-PERT SOLAR CELLS

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ABSTRACT: We present a cost-effective approach for bifacial p-type mc-Si PERT (passivated emitter and rear totally diffused) solar cells. One of the key elements is a co-diffusion without the use of $POCl_3$ and BBr_3 / BCl_3. Both, phosphorous and boron containing silicate glass is deposited on the wafer surfaces at atmospheric pressure by chemical vapor deposition (APCVD). This approach allows diffusions without the need of wafer-spacing. Therefore, the wafers can be in direct contact during the co-diffusion, highly increasing the throughput.
This work demonstrates the feasibility of the described approach based on a comparison to a reference process in which the diffusion is carried out with conventional wafer-spacing.
Sheet resistance and doping profiles do not depend on the position within a stack of 75 wafers and match with the wafers co-diffused with conventional spacing. Despite the direct contact of the wafers during the stacked co-diffusion, no cross-doping was observed. Impurity gettering in stacked co-diffusion is very effective and comparable to the reference process. Finally, a comparison of conventional co-diffused and first stacked co-diffused bifacial p-type mc-Si PERT solar cells is provided.

1 INTRODUCTION

Photovoltaics is on its way to become the most cost-effective option for the production of electric energy. In recent years, the price for Si solar cells steadily declined while the efficiency continuously rose. However, the full potential for cost-efficient solar cells is by no means exhausted yet.

We present a new approach which combines the potential for high efficiencies with lowest production cost, to reach an excellent compromise between both goals. Our idea is to realize a cost-efficient process for bifacial PERT (passivated emitter and rear totally diffused) solar cells and apply it on cost-efficient p-type multicrystalline (mc) silicon wafers which still have a high market share.

One of the key elements of the concept is to get rid of classical diffusion processes which require gaseous $POCl_3$ for phosphorous diffusion and BBr_3 / BCl_3 for boron diffusion. In order to achieve this, dopant containing silicate glasses are pre-deposited at atmospheric pressure via chemical vapor deposition (APCVD). The APCVD system we use is an inline tool which transports the wafers via rollers. Dopant containing glass depositions are made within a few minutes at moderate temperature. The subsequent drive-in only requires heat, N_2 and O_2. An important advantage of the described procedure is the practicability of a co-diffusion without any masking and removal steps which simplifies the otherwise more complex PERT solar cell production process [1]. The applicability of the described APCVD based co-diffusion process on p-type mc-Si was already demonstrated in previous work [2].

The present work goes even one step further and presents another advantage of the co-diffusion based on APCVD glasses. As the dopant containing silicate glasses are deposited prior to diffusion, no spacing is required during the co-diffusion process. As a consequence, wafers can be loaded on top of each other in stacks which allows for an extremely high throughput solution. We present results of a feasibility study with cell precursors and additionally the first stacked co-diffused Si solar cells. Our approach aims for bifacial PERT solar cells, though a stacked co-diffusion could be utilized for most contemporary Si solar cell concepts.

2 SIMULATION

One of the most sensitive factors for impurity gettering and also for emitter diffusion is the temperature. Crystalline silicon is an excellent heat conductor implying that wafers loaded with conventional spacing always show a spatially very homogeneous temperature.

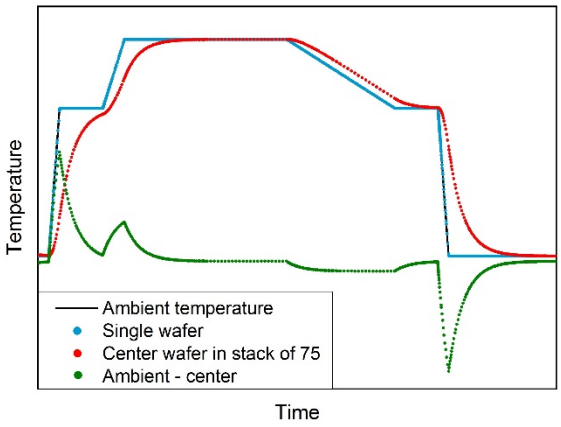

Figure 1: Simulation of the temperature during the co-diffusion step. Wafers loaded with conventional spacing (blue dots) follow the ambient temperature (solid black line) almost instantly. The temperature in the middle of a stack of 75 wafers (red dots) lags behind.

However, in the case of stacked wafers with air between the wafers instead of a good thermal conductor and no high pressure exerted in order to improve the heat transfer, the thermal contact resistance between two wafers is much higher than an equivalent thermal resistance of a wafer in vertical direction. We found no model to parameterize the contact resistance accurately in our case. We therefore performed an experiment where a stack of 49 wafers is heated on a hot plate with a controlled temperature ramp. The plate temperature

underneath the stack as well as the temperature on top of the stack is measured over treatment time by thermocouples.

A simplified setup of this experiment is modeled 2-dimentional with a cylindrical symmetry and the time dependent heat diffusion equation is solved numerically with the finite element simulator flexPDE [3]. We assume a wafer equivalent radius of 8.8 cm (in order to have the same area as a 15.6 x 15.6 cm^2 wafer) and a stack thickness of 7.8 mm (corresponding to 49 wafers). As we are more interested in an average temperature distribution inside the stack rather than on the local temperature variation induced by each wafer interface, we lumped the effect of the thermal contact resistance between wafers in an effective thermal diffusivity value in the vertical direction (D_z) which is one fitting parameter. The diffusivity parameter in the radial direction D_R is set to the value measured for bulk silicon D_R=0.88 cm^2s^{-1} [4]. In this framework, the diffusivity becomes a tensor, which diagonal components are D_R and D_z and the off diagonal terms are zero. The stack surface in contact with the hot plate is modelled by a fixed temperature (Dirichlet) boundary condition where we used the hot plate temperature profile. The other surface is modelled using a convective (Robin) boundary condition where the temperature far away from the surface is set to room temperature, and the surface convection velocity (S) is our second fitting parameter. Fitting the time evolution of temperature in the middle of the wafer at the top surface, an excellent agreement (see Fig. 2) between measurement and simulation is found with D_z=2.6 10^{-3} cm^2s^{-1} and S=2 10^{-4} $cm.s^{-1}$. Note that the ratio of D_R/D_z approaches 300 confirming that the thermal resistance between wafers is dominating the total vertical thermal resistance of the stack heat. However, because the ratio of the diffusion length implied by this ratio of diffusivity ($300^{0.5}$=17) is comparable to the ratio of diameter of the stack to its thickness (8.8x2/0.78=22), the radial and vertical diffusion might be of comparable magnitude. This actually justifies the use of a 2-dimensional simulation for this problem. We originally included a radiative transfer (Stefan-Boltzmann law) additionally to the convective transfer at the free surfaces. We, however, observed no significant difference in the modeled temperature profile with and without radiative transfer, even considering a surface emissivity of 1 (black body), and decided to drop the radiative transfer for simplicity.

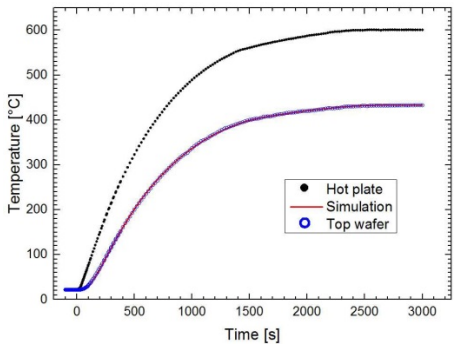

Figure 2: Thermal contact resistance and convection surface velocity evaluation. Black dots represent the temperature of the hot plate, blue open dots the temperature in the center of the top wafer of the stack and the red line is the simulation.

The calibrated simulation is now used to simulate the temperature distribution within a stack of 75 wafers when placed into the oven and exposed to the oven temperature variation. All boundary conditions are then set to convective with ambient temperature far from the boundary set to the measured temperature profile in the oven. The obtained temperature profile for the middle of the stack at the center of the wafer is represented in Fig. 1.

Because of the thermal inertia induced by the contact resistance between wafers, the temperature in the middle of a stack of 75 wafers lags significantly behind the temperature of the oven. Therefore, a short stabilization step before a smooth ramping up to maximum temperature is helpful to minimize this effect.

At higher temperatures, the wafer in the middle of the stack does not significantly differ from a wafer loaded with conventional spacing. Furthermore, the stack may need several minutes after the diffusion process ends to cool-down to room temperature.

3 EXPERIMENTAL

The overall experiment consists of two parts. Prior to solar cell fabrication the impurity gettering efficacy and emitter homogeneity of the stacked co-diffusion was studied with solar cell precursors manufactured similar to the solar cell process using the related flow chart shown in Fig. 3. Afterwards, first stacked co-diffused PERT solar cells were processed using the flow chart shown in Fig. 4.

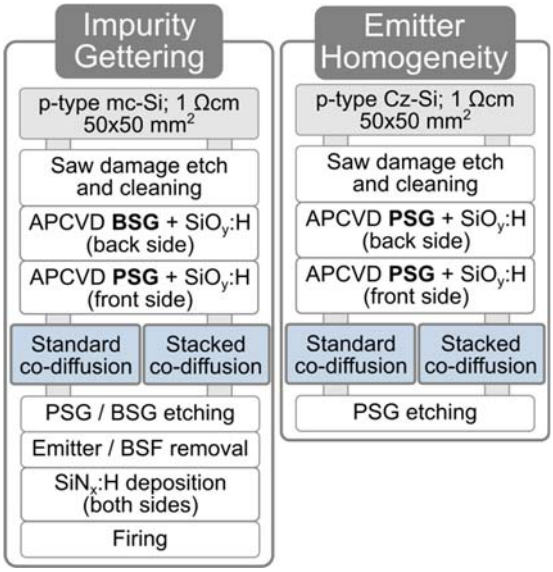

Figure 3: Process flow chart of the solar cell precursors. The precursor production includes the most relevant steps of solar cell production.

The solar cell precursors for the gettering analysis were produced using standard commercial boron-doped (~1 Ωcm) mc-Si (same ingot as used for the PERT cells). Standard commercial boron-doped (~1 Ωcm) Czochralski silicon (Cz-Si) was used to study the emitter homogeneity.

For the gettering study the initially 156x156 mm^2 wafers were laser cut into 50x50 mm^2 pieces. After saw-

damage etch and cleaning, boron-containing silicate glass (BSG) was deposited on the samples for the gettering analysis with the first injector of the roller APCVD system and SiO_2 capped with the second injector in one pass. Afterwards phosphorous-containing silicate glass (PSG) was deposited and capped with SiO_2 on the opposite wafer side in a second pass.

In case of the Cz-Si samples the wafers were also laser cut to 50x50 mm^2 and PSG capped by a SiO_2 layer was deposited on both sides.

Afterwards, three different diffusions with stacks of 75 wafers each were performed to investigate the influences of the peak temperature and ambient conditions. The diffusions differ in terms of peak temperature and N_2/O_2 ratio and are temperature-only steps in each case. After the diffusions the stacks were separated manually. We never observed sticking of wafers in the stack. The APCVD glasses were subsequently removed in diluted HF. Doping profiles of the Cz-Si precursors were investigated via electrochemical-capacitance-voltage measurements (ECV). In case of the mc-Si precursors, the doped layers were etched off and finally the surfaces passivated with PE(plasma-enhanced)CVD SiN_x:H which was fired at 850°C set-temperature. The gettering efficacy was analyzed with the help of excess charge carrier lifetime (τ_{eff}) and interstitial iron concentration ($[Fe_i]$) measurements. $[Fe_i]$ was measured according to the well-established method published by Zoth and Bergholz [5] which was generalized for arbitrary acceptor concentrations and excess carrier concentrations by Macdonald *et al.* [6].

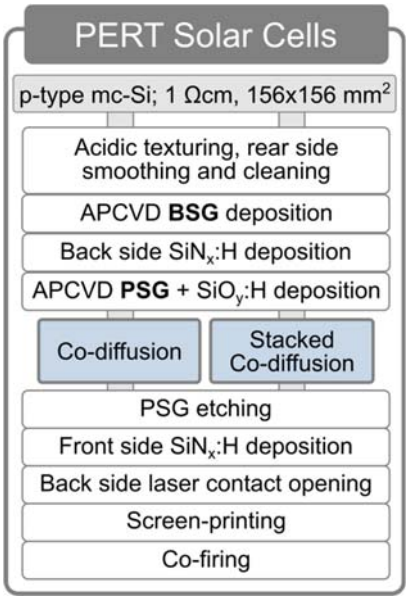

Figure 4: Process flow chart of the bifacial mc-Si p-PERT solar cells in the experiment. After APCVD deposition the wafers were co-diffused in a quartz tube furnace with conventional spacing (control) and in stacks.

For the stacked co-diffused PERT solar cells, standard commercial boron-doped (~1 Ωcm) mc-Si was used. The 156x156 mm^2 wafers are from an outer center brick of a G5 ingot. All wafers chosen are from the same brick but from different positions in height (bottom to top). In the first process step, the saw damage was etched off. Afterwards, the backsides of the wafers were coated with boron-containing silicate glass (BSG) via APCVD. In the next step the BSG was covered with SiN_x:H by remote PECVD. The front sides were coated with PSG and capped with SiO_y:H via APCVD in one pass. At this point, the wafers were divided into two groups. About half of the wafers were conventionally co-diffused to serve as control for the process, the other half was co-diffused in a stack of 50 wafers. In both cases the drive-in was performed in a standard quartz tube furnace in N_2/O_2 ambient. As the dopant containing glasses have been deposited prior to the actual diffusion, neither $POCl_3$ nor BBr_3/BCl_3 was induced. After diffusion, the two groups were further processed together. The PSG/SiO_y:H stack on the front was etched off and PECVD SiN_x:H deposited afterwards. The backside BSG/SiN_x:H stack remains on the wafers for surface passivation and had to be laser contact opened in the next step. Finally, the contacts on the front and backside were screen-printed and co-fired. The finished solar cells were IV-measured using a cetisPV tool from HALM.

4 RESULTS AND DISCUSSION

4.1 Impurity Gettering

The feasibility of a co-diffusion for PERT solar cells from previously deposited APCVD BSG and PSG was already demonstrated by Fellmeth *et al.* [7]. We have proven the practicability of a similar co-diffusion process using p-type mc-Si [2]. To take the next step, a stacked co-diffusion from APCVD glasses, we conducted a pre-experiment in which the gettering efficacy and emitter homogeneity of stacked diffused solar cell precursors was studied.

The mc-Si wafers for the gettering precursors are taken from the same G5 ingot used for the PERT solar cells, but from an edge brick. The outer fringe of not yet gettered mc-Si edge bricks features high amounts of metal impurities like iron (Fig. 5, top) which makes it interesting for gettering studies. The presented experiment includes five as-grown samples which were only chemically cleaned and surface passivated. The measured $[Fe_i]$ of the as-grown samples are in the range of 2-3x10^{12} cm^{-3}. The three different conventional and stacked co-diffusions in the experiment removed significant amounts of $[Fe_i]$, especially in the upper part of the samples. The “red” zone in the upper part of the samples is completely removed in each case. The co-diffusion gettering with 840°C peak temperature reduced the $[Fe_i]$ to 7-9x10^{11} cm^{-3}. The two co-diffusions in the experiment with 870°C and different ambient conditions were even more effective and resulted in $[Fe_i]$ within a range of 6-7x10^{11} cm^{-3}. The $[Fe_i]$ maps displayed in Fig. 5 show exemplarily results of one of the co-diffusions with 870°C peak-temperature. The measured mean values of all mc-Si precursors in the co-diffusion are shown in the lower part of the figure. The values of the stacked diffused samples are plotted against their position in the co-diffused stack of 75 wafers. Both, the standard and stacked co-diffusion reduced the amount of Fe_i in the samples significantly, though the standard co-diffusion is slightly more effective. A correlation between the position within the stack and the Fe_i reduction cannot be observed.

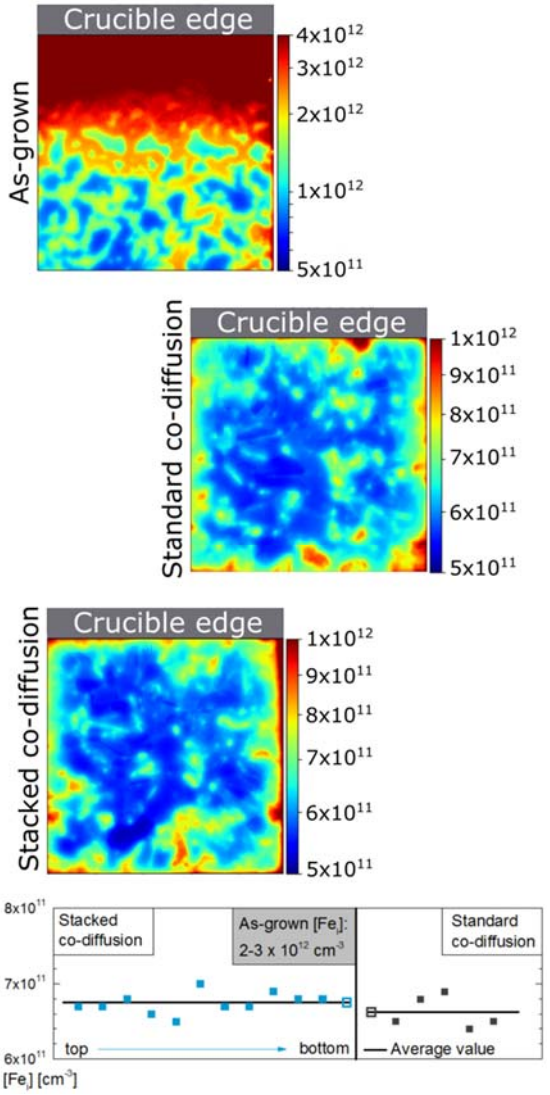

Figure 5: Fe_i concentrations of as-grown, standard co-diffusion gettered and stacked co-diffusion gettered (stack of 75 wafers) samples from a mc-Si edge brick.

Similar behavior is seen in the τ_{eff} measurement results. The as-grown samples are in the range of τ_{eff} = 7-10 µs (harmonic average). After gettering the average τ_{eff} of all stacked co-diffused samples increased to more than 230 µs and the average of all standard co-diffused samples to more than 250 µs (Fig. 6).

Overall, it can be concluded that the position within a stack of 75 wafers is not relevant for the gettering efficacy. Furthermore, gettering for stacked co-diffused samples works similar though slightly less effective as for samples diffused with standard spacing.

4.2 Emitter Homogeneity

The doping profiles displayed in Fig. 7 show a nearly perfect match between conventionally diffused reference samples and stacked diffused samples for all three diffusions in the experiment. Moreover, the position within the co-diffusion stack (bottom, middle or top) does not have any influence on the doping profiles.

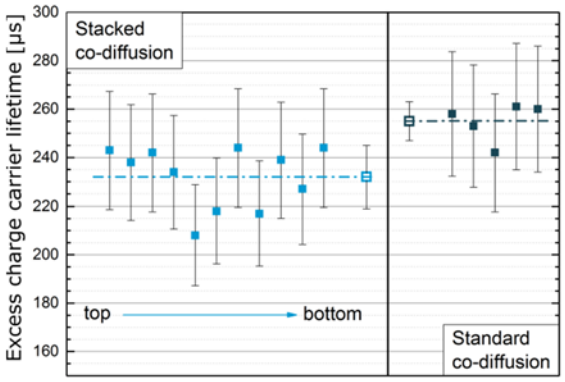

Figure 6: Excess charge carrier lifetime of mc-Si samples after co-diffusion gettering with conventional spacing (right) and in a stack of 75 wafers (left).

The difference between ambient 1 and ambient 2 is the N_2/O_2 ratio, while the overall flow in both ambient mixtures is the same. With a peak-temperature of 870°C, the diffusion with the higher O_2 concentration (ambient 1) resulted in slightly higher dopant concentrations. This came to no surprise for the reference wafers with standard spacing but was not expected for the stacked co-diffusion. Oxygen in phosphorus diffusion ambient atmospheres enhances the diffusion [8], however, the wafer surfaces in a stack are not directly exposed to the ambient but face neighboring wafer surfaces. Therefore, the wafers in the stack were not expected to show influences of varying ambient conditions which nevertheless is apparently the case.

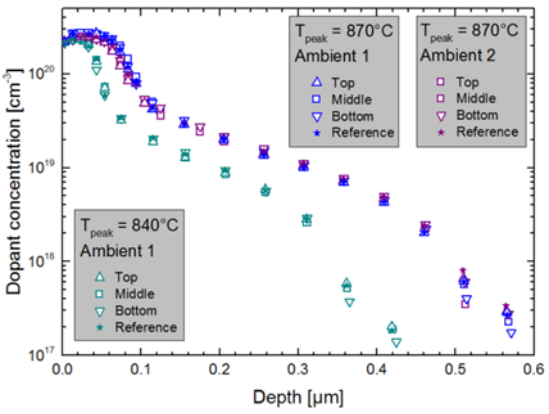

Figure 7: Comparison of phosphorous emitter doping profiles. Precursors diffused in stacks of 75 wafers and conventionally diffused solar cell precursors do not show any significant differences. The higher diffusion temperature results in deeper profiles.

4.3 PERT Solar Cells

After the successful pre-tests, first stacked co-diffused bifacial mc-Si p-PERT solar cells were produced. A qualitative comparison of the solar cell parameters is presented in Fig. 8.

All values are normalized to the average values of all solar cells in the experiment. So far, the stacked co-diffusion seems to perform as good as the conventional co-diffusion. However, the optimization of the processes is currently still in progress. The results presented here show the first try.

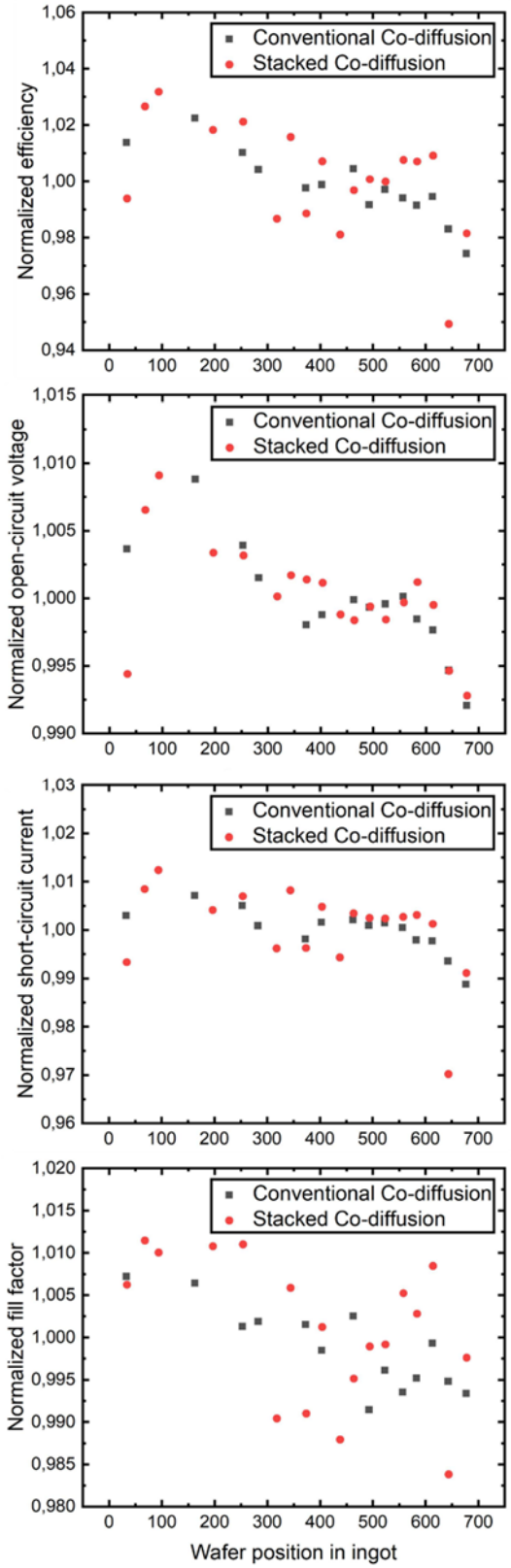

Figure 8: Normalized efficiency, open-circuit voltage, short-circuit current and fill factor of stacked- and standard co-diffused p-type mc-Si PERT solar cells against the height of the wafer in the mc-Si ingot.

Each parameter in Fig. 8 is plotted vs. the wafer height position in the ingot column. As the pre-experiment showed no correlation of gettering and emitter diffusion to the wafer positon within the stack during the co-diffusion, the stack sequence of the wafers in the solar cell process was randomized. All four parameters presented in Fig. 8 show a dependency on the height position of the wafer within the ingot. Thanks to the randomization of the stack sequence and the pre-experiment, the stack sequence cancels out as possible reason. The grain size increases from bottom to top as well as the impurity concentration due to segregation during ingot growth and the density of defect clusters. Note that the material used is standard mc-Si, not high performance material. Both, grain boundaries and impurities act as recombination sites. Apparently, the impurity concentration and the density of defect clusters are more detrimental than the overall length of the grain boundaries (at least for wafer positions in the brick >200).

5 SUMMARY

The influence of a stacked co-diffusion process using doping layers deposited via APCVD was analyzed concerning gettering efficacy, emitter homogeneity and solar cell performance.

The simulation of the temperature of a stacked co-diffusion indicated a lag behind compared to a co-diffusion with standard spacing. By including a stabilization step before ramping up to maximum temperature, the deviation at temperatures relevant for gettering and emitter diffusion can be significantly decreased.

In the gettering experiment it could be shown that Fe_i was gettered similar in co-diffusions with standard spacing and stacked co-diffusions. The stacked co-diffusion gettering worked without any identifiable dependency on the position within the stack of 75 solar cell precursors. The phosphorous emitter doping profiles of conventional and stacked co-diffusions were found to match. The position within the stack does not play a role, too. Higher O_2 concentrations during co-diffusion were found to increase the dopant concentrations even in stacked co-diffusion were the wafer surfaces are not directly exposed to the ambient conditions.

Not any of the three different co-diffusions in the pre-experiment resulted in a sticking of the wafers. In all cases the stack of wafers needed several minutes to cool down to room temperature.

A proof-of-concept of the stacked co-diffusion from dopant containing APCVD glasses for bifacial p-type mc-Si PERT solar cells was already successful. However, the optimization of cell process is currently still ongoing.

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