STACKED PECVD BACKSIDE DIELECTRICS: AN OPTION FOR A FIRING STABLE PASSIVATION OF INDUSTRIAL TYPE SCREEN-PRINTED SILICON SOLAR CELLS

Sebastian Joos, Uwe Heß, Sven Seren, Barbara Terheiden, Giso Hahn
University of Konstanz, Department of Physics, P.O. Box, 78457 Konstanz, Germany
Email: sebastian.joos@uni-konstanz.de, Phone: +49 7531 88 2088, Fax: +49 7531 88 3895

ABSTRACT: On the way to higher efficiencies and reduced costs material quality has to increase while wafer thickness decreases. With industrial screen-printed Cz solar cells reaching above 19% efficiency [1] the well-established Al-BSF is a limiting factor for further improvement. Simple and cost effective to deposit dielectrics with good characteristics for backside passivation have to be found. Our approach is a multilayer stack-system consisting of amorphous silicon carbide (SiC_x), silicon oxide (SiO_2) and silicon nitride (SiN_x). This system enables us to achieve a low surface recombination velocity of 7.6 cm/s although a transparent SiC_x layer with high carbon content (CH_4/SiH_4 flow rate of 8) is used. SiC_x passivates n- and p-doped silicon at high deposition rates and low deposition temperatures. The cross compatibility of the used dielectrics enables us to deposit the stack system within one deposition step.
Keywords: PECVD, passivation, silicon carbide

1 INTRODUCTION

The rear side passivation of a standard industrial solar cell is provided by an aluminum back surface field. As the passivation quality of the Al-BSF is limited to around 200 cm/s, apart from a B-BSF dielectric passivation layers are the first choice for a replacement. SiN_x (silicon nitride) being the de facto standard for front side dielectrics is based on a strong field effect passivation as a result of built-in positive fixed charges. However, it is not well suited as a backside passivation of the p-doped base material. Results of Dauwe et. al. [2] show that this is mainly due to a parasitic shunt resistance across a floating junction. Already small shunts reduce J_{sc} and thus cell performance noticeably. Another drawback of SiN_x applied as a backside dielectric is the reduced passivation quality for low injection levels. Typically the injection levels are one or two orders of magnitude lower than on the front surface [2].

Thus, dielectrics with good characteristics for backside passivation have to be found. Based on the work of [3] and [4] our approach is a multilayer stack-system with amorphous silicon carbide (SiC_x) as a primary passivation layer.

Amorphous silicon carbide can be deposited in a wide variety of stoichiometries. Beginning with low carbon content the characteristics are quite similar to amorphous silicon in terms of passivation, absorption and temperature stability. At higher carbon contents, the passivation quality drops as the absorption does but the thermal stability increases.

In this work we present a multilayer stack-system consisting of amorphous silicon carbide (SiC_x), silicon oxide (SiO_2) and silicon nitride (SiN_x) aiming at high minority carrier lifetime at high temperatures.

A variation of CH_4/SiH_4 flow rates and thicknesses of SiC_x layers is investigated.

2 MOTIVATION

As we intend to increase thermal stability, a stacked system containing of SiN_x on top of SiC_x is used as a starting point. The first samples, however, show huge improvements in passivation quality (from 250 µs to 1 ms minority carrier lifetime for a CH_4/SiH_4 flow rate of 5), and heavy blistering and delamination of the upper layer after a high temperature annealing step (Figure 1).

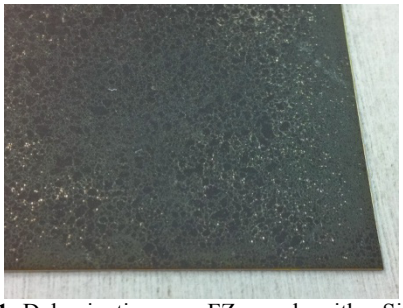

Figure 1: Delamination on a FZ sample with a SiC_x/SiN_x stack after a high temperature firing step.

As described by [4] the blistering seems to be due to hydrogen that is drained into the interface between carbide and silicon. The delamination is due to the fact that the SiC_x layer gets thinner [4] when exposed to high temperatures and due to different thermal expansion coefficients. But the so far known drop in passivation quality with higher carbon contents is reduced.

To deal with blistering and delamination a thin layer of silicon oxide is deposited in between the SiC_x and SiN_x layer. SiO_2 is known to be very elastic at higher temperatures and hence provides the ability to tie the two other layers together. Another positive effect is the ability to absorb excess hydrogen in the built up interface.

3 EXPERIMENTAL DETAILS

For the experiments p-type float zone (FZ) wafers of 2 Ωcm and p-type mc wafers of 0.7 Ωcm resistivity are used (thickness: FZ: 525 µm and 250 µm, mc: 270 µm). After laser cutting and labeling all samples received a CP damage etch (~20 µm each side) followed by RCA cleaning. The chemical oxide which grows during the RCA cleaning step was removed directly before each deposition. SiC_x, SiO_2 and SiN_x layers were deposited on both sides of the wafers in a lab-type PECVD setup (Oxford Instruments Plasmalab System 100). As there is no evidence for cross contamination the complete stack could be deposited within one deposition at a constant temperature. Minority charge carrier lifetimes were measured using the QSSPC (Quasi Steady State Photo-Conductance decay) technique with a WCT-120 photoconductance tool from Sinton Instruments, Inc. For comparison, lifetimes were measured at an injection level of 1E15 cm^{-3}. For selected samples the more relevant injection levels for backside passivation (1E14 cm^{-3}) will be presented as well.

For a comparison of the $SiC_x/SiO_2/SiN_x$ stack with SiC_x alone and SiC_x capped by SiO_2, all depositions were made within one day with the exact same pretreatment and equally long process times. The deposition temperature was 350°C. For the annealing tests the C-rich silicon carbide layer was deposited using a flow rates of 8 parts CH_4 to 1 part SiH_4. After deposition, the samples were annealed at 400°C for 30 Minutes in N_2 atmosphere. For thermal stability tests the C-rich silicon carbide layer was deposited using flow rates of 17 parts CH_4 to 1 part SiH_4. After deposition, the samples were fired @ 800°C peak temperature (2 s). Figure 2 shows an overview of the process steps.

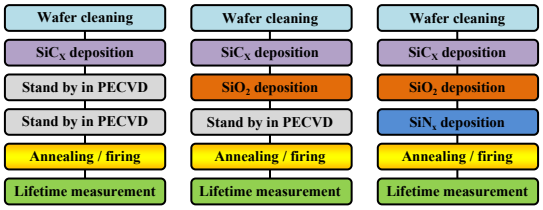

Figure 2: Stack system comparison process flow.

The deposition time for the $SiC_x/SiO_2/SiN_x$ stack system is less than 5 minutes.

4 RESULTS

4.1 Influence of capping layers on SiC_x

To verify the positive effect of the additional layers SiO_2 and SiN_x in the stack systems we start with a comparison of the $SiC_x/SiO_2/SiN_x$ stack system with SiC_x alone and SiC_x capped by SiO_2.

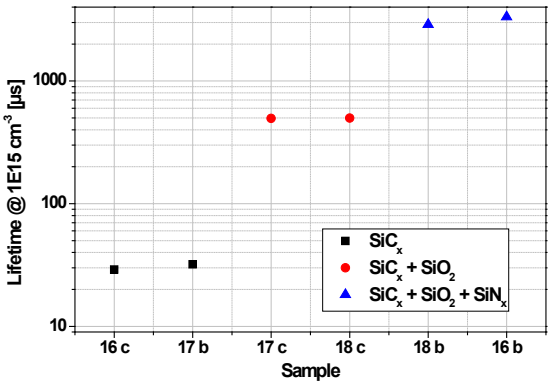

Figure 3: Comparison of a $SiC_x/SiO_2/SiN$ stack system, SiC_x alone and SiC_x capped by SiO_2 on 525 µm FZ-Si.

Figure 3 shows that SiC_x alone with minority charge carrier lifetimes between 20 and 23 µs is far away from being a good passivation layer and needs to be further optimized. Other publications reported significantly higher lifetimes at high CH_4/SiH_4 ratios [5]. But even this low lifetime SiC_x shows in a stack system an impressive minority charge carrier lifetime of 3.3 ms (3.0 ms at 1E14 cm^{-3}). Assuming an infinite bulk lifetime, this translates to a surface recombination velocity of just 7.6 cm/s (8.4 cm/s at 1E14 cm^{-3}). As also observed by [4] the stack with SiO_2 capping shows already a large improvement in lifetime (500 µs) compared to the SiC_x single layer samples.

Another fact is the influence of a growing native oxide. Although the duration in which the samples are exposed to air is a minute there are obvious gains for the samples with less time after the HF Dip. The work by Janz et al. [6] also showed this behavior for SiC_x layers on longer time scales.

4.2 Stack variations annealed

In the following study we compared the lifetimes of FZ and mc samples deposited with different CH_4/SiH_4 ratios and thicknesses. Figure 4 and Figure 5 show maximum lifetimes measured during stepwise annealing in N_2 atmosphere.

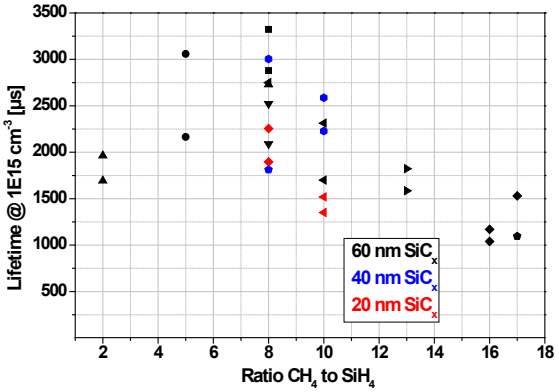

Figure 4: Maximum lifetimes on 525 µm FZ-Si samples ($SiC_x/SiO_2/SiN_x$ stack) over the CH_4/SiH_4 ratio.

With lifetimes peaking around CH_4/SiH_4 flow rates of 8, Figure 4 shows an interesting behavior of the stacked passivation system. Where SiC_x shows its best passivation quality for lowest carbon contents [3] the stack maxes out at medium carbon contents around ratios

of 8. This is a hint for a complex interaction between the incorporated layers that is rather based on the chemical composition of the SiC_x layer than on the passivation quality of it.

Variation of the SiC_x layer thickness shows an optimum between 40 and 60 nm. Thicker layers are not used because the mechanical stability is influenced. Here blistering, delamination and cracks become more likely. As the average lifetime only slightly decreases with thickness the mechanical stability during annealing steps should be the selection criterion for layer thickness. So far, the SiO_2 and SiN_x layers are not optimized in terms of passivation quality but only in terms of mechanical stability.

First tests on multicrystalline wafers show the good passivation quality of the stack for this material (Figure 5). We conclude that the high amount of hydrogen in the SiC_x layer supports the bulk passivation as SiN_x reference wafers show less than 100 µs lifetime.

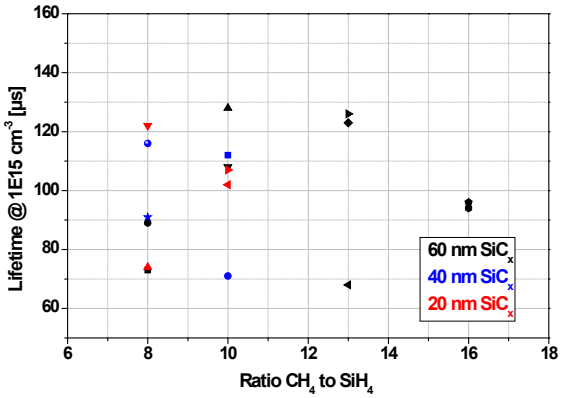

Figure 5: Maximum lifetimes on mc samples over the CH_4/SiH_4 ratio.

With the data for mc-Si samples from Figure 5 it seems that the maximum in lifetime is even further pushed to higher CH_4/SiH_4 ratios. Although for a clear conclusion more samples have to be processed here as the deviations are quite significant. The influence of layer thickness is again less pronounced.

4.3 Thermal stability

For our firing tests an industrial-type belt furnace from Centrotherm was used. The given temperatures are measured wafer temperatures from pre-tests and not set-point temperatures. The samples were fired on SiN_x coated dummy wafers to avoid a contamination from the metal belt.

We started with a variation of the CH_4/SiH_4 ratio and thicknesses which provided mechanical stability after firing. The firing temperature was reduced because our lifetime samples were not metalized. This fact leads to material temperatures up to 80°C higher than on metalized cells. Figure 6 shows the results from firing tests performed for 2 s above 800°C.

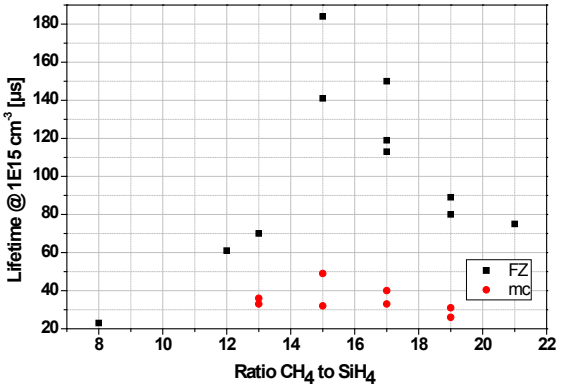

Figure 6: Lifetime of FZ (250 µm) and mc samples after a firing step for 2 s above 800°C peak temperature.

Compared to our colleagues work [5] based on SiC_x from a different PECVD system we had to move towards much higher CH_4/SiH_4 flow rates of 15 to maintain a reasonable surface passivation of 65 cm/s (105 cm/s for 1E14 cm^{-3}) on FZ material after firing. Glunz et al. [7] showed that such a performance allows high open-circuit voltages. The surface recombination velocity of the mc-Si samples is below 200 cm/s (250 cm/s at 1E14 cm^{-3}). Assuming a cell with LFC back contacts with 2% coverage these values lead to an effective surface recombination velocity of < 200 cm/s for FZ material and < 350 cm/s for mc-Si [8]. In the case of FZ-Si the passivation can compete with an Al-BSF which is in the range of 260 - 700 cm/s [9], furthermore a stack system has the benefit of an improved backside reflection [7].

The influence of capping layers on thermal stability is shown in Figure 7 for a CH_4/SiH_4 flow rate of 17.

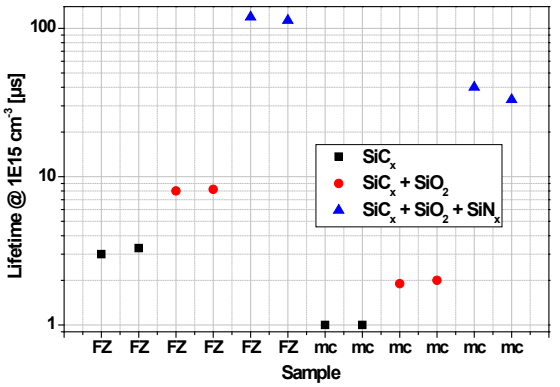

Figure 7: Comparison of a $SiC_x/SiO_2/SiN_x$ stack, SiC_x single layer and SiC_x capped by SiO_2 fired above 800°C peak temperature.

Figure 7 again shows that the SiC_x layer has to be optimized, especially with regard to thermal stability. But as expected, the addition of SiO_2 and SiN_x improves thermal stability of the passivation for FZ and mc material. Our future work is expected to show if the implementation of the stack is beneficial in a traditional solar cell concept with a firing step after stack deposition or if an adapted cell concept without firing the rear side passivation is the better choice. So far, first cell results on the multicrystalline silicon ribbon material RGS (Ribbon Growth on Substrate) [10] with a fired carbide rear side passivation showed an improved cell performance.

5 SUMMARY

With the results achieved so far, we conclude that a dielectric stack system involving silicon carbide as a primary passivation layer is a promising way for surface passivation. Our transparent stack system showed a very good surface passivation with minority charge carrier lifetimes above 3.3 ms on 2 Ωcm FZ samples. On the one hand the backside of p-type cells could be improved as shown by [4] and [5]. Calculated effective surface recombination velocities for fired FZ samples with LFC contacts below 200 cm/s and the improved backside reflection of a transparent stack system are promising properties for tests on cell level. On the other hand an improvement of the front side of n-type cells should be possible as the used carbide layers in the stacked system show a low absorption. These facts in combination with high deposition rates (the whole stack system in less than 5 minutes), cost effective precursors and the possibility to deposit the whole stack in one chamber at a constant and low deposition temperature shows the potential of this approach as an industrially used dielectric.

ACKNOWLEDGEMENTS

Part of this work was funded by the BMU in the OP-RGS (0325056) project. The content of this publication is the responsibility of the authors.

6 REFERENCES

[1] A. Dastgheib-Shirazi, H. Haverkamp, F. Book, B. Raabe and G. Hahn, *Investigations of high refractive silicon nitride layers for etched back emitters: Extended surface passivation for Selective Emitter ConcepT cells (SECT),* Proc. 24th EU PVSEC, Hamburg, 2009.

[2] S. Dauwe, L. Mittelstädt, A. Metz, and R. Hezel, *Experimental evidence of parasitic shunting in silicon nitride rear surface passivated solar cells*, Progress in Photovoltaics: Research and Applications, **10**, 2002, pp. 271-278.

[3] S. Riegel, B. Raabe, M. P. Stewart, P. Borden and G. Hahn, *Thermal stability of PECVD a–$Si_{1-x}C_x$ layers for crystalline silicon solar cell passivation,* Proc. 24th EU PVSEC, Hamburg, 2009.

[4] S. Janz, *Amorphous Silicon Carbide for Photovoltaic Applications*, Thesis, Verl. Dr. Hut, 2006.

[5] S. Riegel, B. Raabe, R. Petres, S. Dixit, L. Zhou, G. Hahn, *Towards higher efficiencies for crystalline silicon solar cells using SiC layers*, Proc. 23rd EU PVSEC, Valencia, 2008.

[6] S. Janz, D. Suwito, S. W. Glunz, *Passivation mechanisms of amorphous SixC1-x layers on highly doped and textured Si surfaces*, Proc. 22nd EU PVSEC, 2007.

[7] S. Glunz, S. Janz, M. Hofmann, T. Roth, and G. Willeke, *Surface Passivation of Silicon Solar Cells using Amorphous Silicon Carbide Layers*, 4th WCPEC, 2006, pp. 1016-1019.

[8] D. Kray, *Hocheffiziente Solarzellenstrukturen für kristallines Silicium-Material industrieller Qualität*, Thesis, 2004.

[9] S. Riegel, S. Gloger, B. Raabe, and G. Hahn, *Comparison of the passivation quality of boron and aluminum BSF for wafers of varying thickness*, 24th EU PVSEC, 2009.

[10] U. Heß, S. Joos, S. Seren, G. Hahn, T. Weber, A. Schönecker *Dielectric Rear Side Passivation on Ribbon Growth on Substrate (RGS) Solar Cells,* submitted to 25th EU PVSEC, 2010.