Preprint

Investigation of Contact Resistivities on APCVD (p) Poly-Si for Fired Passivating Contacts

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Abstract. We investigate the properties of boron doped polycrystalline Si (poly-Si) deposited by atmospheric pressure chemical vapor deposition (APCVD) applied to fired passivating contacts (FPC), where no high temperature annealing takes place apart from the contact firing step. X-ray diffraction measurements show that the APCVD poly-Si is already partially crystallized directly after deposition and the crystallite size further increases during firing. Without metallization an implied open circuit voltage of up to 719 mV is achieved. Screen-printing with an Ag paste yields minimal contact resistivities of down to 1 mΩcm² at high firing temperatures. Furthermore, thicker poly-Si layers, accomplished by driving the same wafer multiple times through the APCVD system, generally correspond to lower contact resistivities for the FPC. This can partly be explained by an increasing crystallinity and conductivity during deposition due to the higher thermal budget during deposition for thicker layers as well as by a larger contact area for thicker poly-Si layers. Scanning electron microscopy on sample cross-sections show that almost the entire poly-Si layer is covered with Ag crystallites at high firing temperatures. For lower temperatures a lower density of Ag crystallites in the poly-Si is visible. Both findings hold for planar and textured surfaces.

**Keywords:** (p) Poly-Si, FPC, APCVD, Metallization

1. Introduction

Passivating contacts, based on polycrystalline Si (poly-Si) and a thin interfacial SiO_X layer, enable high conversion efficiencies due to their ability to combine excellent charge carrier selectivity and passivation quality underneath the metal contacts [1], [2]. Most established processes require at least one extended annealing step at high temperatures for crystallization after amorphous silicon (a-Si) deposition, even when using in-situ doping, as is done in this work as well. However, the fired passivating contact (FPC) approach simplifies the process flow. Thereby, the thermal budget is significantly reduced, ideally featuring only one fast firing step, which combines metallization, dopant activation, partial crystallization, and hydrogenation [3]. A good passivation quality was already shown previously for plasma-enhanced chemical vapor deposition (PECVD) as well as atmospheric pressure chemical vapor deposition (APCVD) a-Si [3], [4], [5]. In contrary to PECVD, APCVD enables a high throughput and completely blister-free poly-Si without any additional steps, such as annealing before SiN_X:H deposition [3]. In this experiment APCVD (p) poly-Si is investigated, which has proven to be more challenging to obtain similarly low contact resistivities as for (n) poly-Si [6], [7], [8]. In the following, we will demonstrate a successful, low ohmic contact formation by the FPC approach. The passivation after metallization has not yet been investigated.

2. Methods

n-type (5 Ωcm) Cz-Si wafers with a size of 156.75x156.75 mm² and a thickness of 150 µm were saw damage etched by KOH at 80°C. Furthermore, a group of samples afterwards was treated with an alkaline texture before all samples were subsequently exposed to wet chemical cleanings with ozone and piranha solutions. A thin SiO_X layer (~1.7 nm) was grown by thermal oxidation in a tube furnace. In the following, only boron doped poly-Si was deposited on one side using an APCVD tool from SCHMID by adding the precursor B_2H_6 to the SiH_4 flow [5]. Different thicknesses of ~60, ~120, and ~180 nm, determined by scanning electron microscopy (SEM), were realized by driving the same wafer multiple times through the APCVD system with the same belt speed. For 120 nm thick poly-Si, additionally reference samples were crystallized in a tube furnace at 920°C for 30 min to realize the high temperature passivating contact (HTPC) approach. For hydrogenation a ~75 nm thick SiN_X:H layer was deposited on both sides using PECVD. A fire-through Ag paste was screen-printed in patterns suitable for the application of the transfer length method (TLM) with finger widths of 40, 50, and 60 µm, respectively. The contact formation was carried out in a conventional fast firing belt furnace at five different set peak firing temperatures (T_{SPF}) between 790-890°C. The contact resistivity (ρ_C) was evaluated by TLM measurements, using a pv-tools setup. To evaluate the behavior of the Ag paste, cross-sections of the metallized samples were examined by SEM after ion milling. Since the passivating contact layer stack was only implemented on the front side, the back side was for some samples passivated with an AlO_X/SiN_X:H layer stack (2 fA/cm^2) to evaluate the passivation quality via photoconductance decay (PCD) using a Sinton lifetime tester. X-ray diffraction (XRD) measurements were performed with a Bruker Advance D8 using the grazing incidence method and at an incidence angle of $\omega = 5°$ to determine the crystallite size via the Scherrer equation [9].

3. Results

The non-metallized reference samples in Fig. 1 (left) show high implied open circuit voltage (iV_{OC}) values of up to 719 mV for a 60 nm thick poly-Si layer. These values are obtained by averaging two 5x5 samples each and thus should serve as a trend line. Thinner layers lead to higher iV_{OC} values throughout all firing temperatures. With 180 nm thick poly-Si layers an iV_{OC} above 710 mV is achieved, although a strong temperature dependence is visible with a maximum at T_{SPF} of 865°C. This thickness and temperature dependence suggests that the hydrogen released from the SiN_X layer during firing is of utmost importance for the passivation of the poly-Si/SiO_X interface. Similarly, the reference sample produces an iV_{OC} of 720 mV after firing at 790°C and thus is comparable to the best values of the FPC approach. The a-Si is characterized in its as-deposited and crystallized state via XRD measurements on planar samples, and the crystallite size is evaluated for the (111) poly-Si peak at 29°. These measurements are shown for 120 nm thick layers in Fig. 1 (right) for the as-deposited state and after firing at 790°C and 890°C, respectively, as well as for a HTPC sample. One can see that the a-Si in its as-deposited state is already at least partially crystalline, as is indicated by the small XRD peaks. Furthermore, it is visible that the structure of the poly-Si changes during firing indicated by the higher XRD peak for higher firing temperatures. Extended annealing leads then to an even more apparent change in crystal structure. An evaluation of the crystallite size yields an average crystallite size of just 8 nm in the as-deposited state, of 13.8 nm after firing at 790°C and up to 19 nm at 890°C for planar samples. For the samples after crystallization in the tube furnace at 920°C for 30 min, crystallites up to 30 nm grow. This shows that the APCVD (p) poly-Si already achieves a significant crystallinity by the short temperature exposure of deposition and fast firing, which is only slightly increased by a long annealing step (30 min). It is expected by the authors that the crystalline fraction behaves similar to the crystallite size. However, it was not possible to determine this, as these poly-Si layers are too thin to conduct Raman measurements due to the background interference from the c-Si substrate.
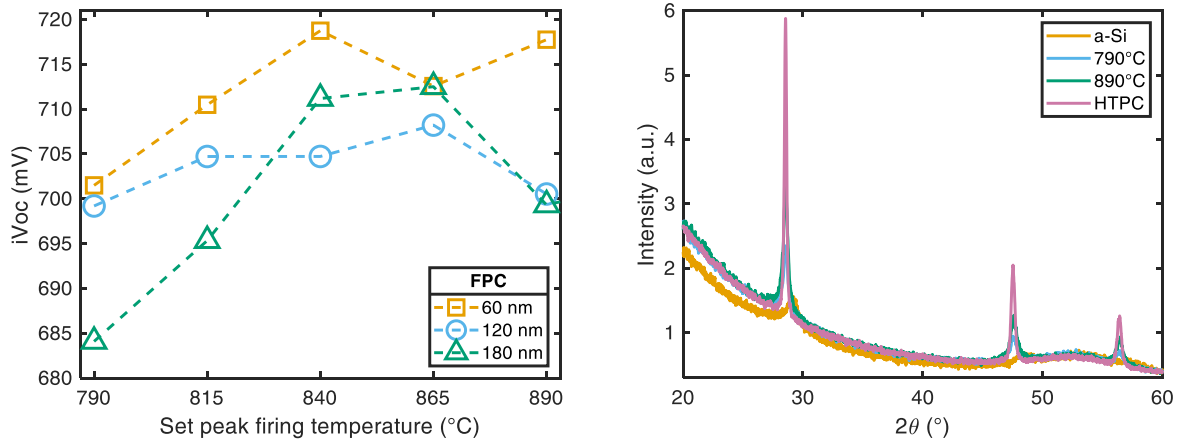
Figure 1. (left) iV$_{OC}$ measurements for non-metallized FPC reference samples at different set peak firing temperatures and thicknesses. (right) XRD measurements for different annealing conditions for the 180 nm thick poly-Si layer.

The results of TLM measurements for 120 nm thick poly-Si are shown in Fig. 2 (left) for FPC and HTPC samples, where the error bar is determined through standard deviation. A similar trend is visible for both processes, that is a decreasing ρ_C with increasing firing temperature. For the HTPC samples, ρ_C reaches its minimum at 4 mΩcm² at the highest firing temperature of 890°C. The FPC samples show even lower contact resistivities of down to 1 mΩcm² at 865°C. The error due to standard deviation of the individual measurements is rather small, underlining the validity of this result. The experiment is also repeated with a wet-chemical interfacial oxide, resulting in similar values. Comparably low contact resistivities are found for a planar wafer substrate in Fig. 2(left). Here, an average contact resistivity below 1 mΩcm² is found at the highest firing temperature. However, for lower firing temperatures no contact resistivities can be measured via TLM which could be due to the higher actual wafer temperature during firing for textured surfaces compared to planar ones. These findings demonstrate the potential of FPC for (p) poly-Si applications in passivating contacts, especially in direct comparison with the commonly used long crystallization process durations.
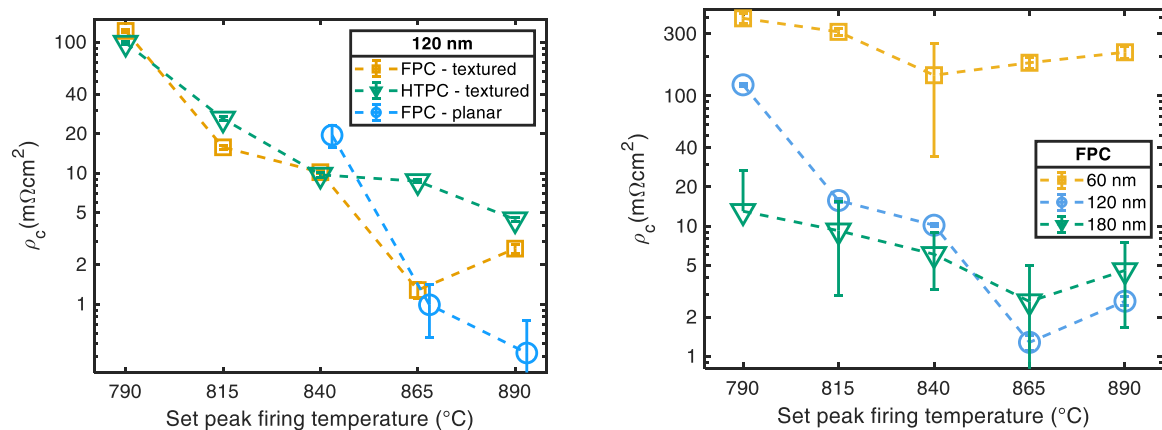

Figure 2. (left) Comparison of contact resistivities between textured FPC and HTPC samples depending on firing temperature, as well as a comparison to a planar sample. (right) ρ_C for textured FPC samples depending on firing temperature for different thicknesses.

Fig. 2 (right) shows that thicker (p) poly-Si also generally leads to a lower ρ_C for most of the firing temperatures. The samples with thicknesses of 120 and 180 nm show a minimum ρ_C of ~1 and ~3 mΩcm², respectively, at a firing temperature of 865°C, while the thinnest layer only yields ρ_C values above 100 mΩcm² and thus significantly higher values than for the thicker poly-Si layers. For lower firing temperatures, ρ_C increases sharply. The thickness dependence

is well described in literature for both (p) poly-Si [7], [8] as well as (n) poly-Si [10] passivating contacts, although a clear explanation is not given.

In Fig. 3, SEM images are shown after ion milling of the sample in cross-section view. At high T_{SFP} of 890°C a significant part of the poly-Si layer is refilled by Ag crystallites. Particularly in the valleys of the pyramids, the Ag crystallites occur only within the poly-Si layer, while at the tips the crystallites also penetrate into the base. This is true for all investigated (p) poly-Si layer thicknesses in Fig. 3(a/b/c). For planar surfaces, as is visible in Fig. 3(d), the crystallite density is similarly high, with crystallites located only in the first or second poly-Si layer and clearly stopping at the interfaces of the poly-Si layer. Thus, the etching behavior and Ag crystallite formation of an Ag paste does not differ much between (p) poly-Si and (n) poly-Si passivating contacts [11]. From this behavior it follows that the contact area between the poly-Si and the Ag crystallites is larger for thicker poly-Si layers, thus reducing the contact resistivity. Another possible suggestion for the lower ρ_C achieved using thicker layers is a different doping height on the wafer surface for different poly-Si thicknesses, which could be due to multiple drive-throughs of the same wafer during deposition at 700°C. This could lead to an accumulation of boron atoms at the wafer surface, correspondingly decreasing the contact resistivity. Furthermore, these multiple drive-throughs can increase crystallinity and conductivity of the poly-Si layers itself. For lower temperatures, as shown in Fig. 3(e/f) for 790°C, almost no Ag crystallites are visible in the poly-Si layer for planar and textured surfaces, explaining the high contact resistivities at these temperatures. Analyzing those SEM images, no significant differences were observed between the HTPC and the FPC samples.
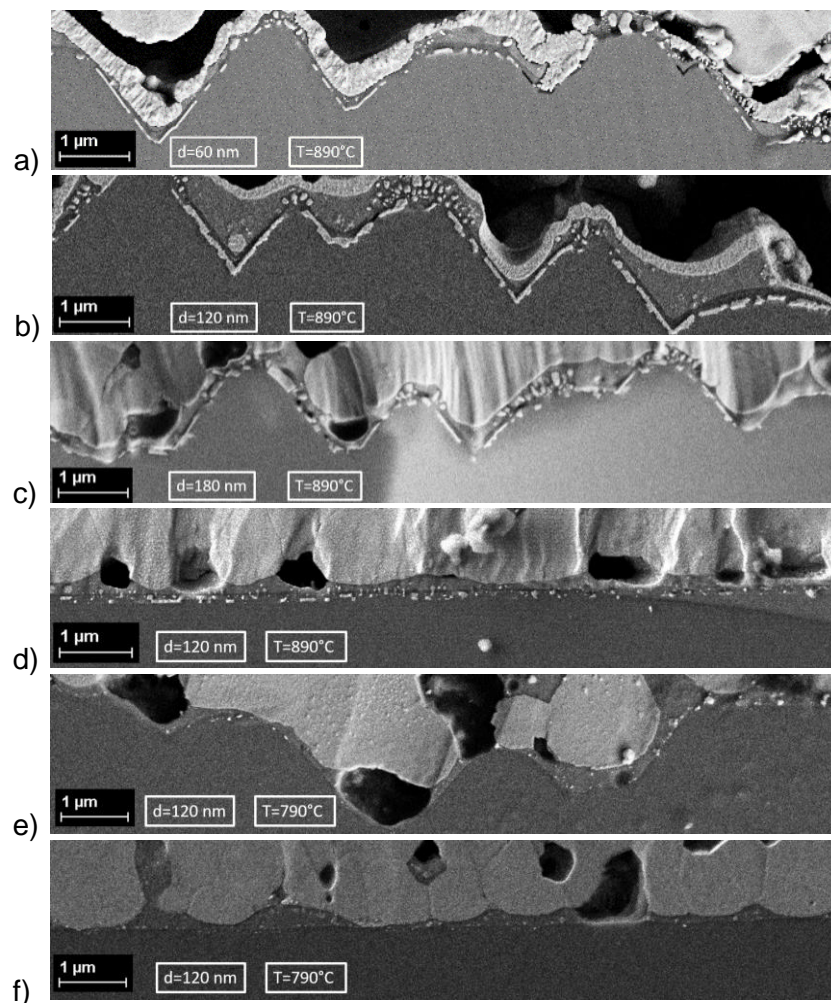
Figure 3. SEM cross-sections after ion-milling. Textured samples fired at 890°C set temperature with a poly-Si thickness of (a) 60 nm, (b) 120 nm, (c) 180 nm, and (d) 120 nm on a planar substrate. 790°C set firing temperature on a (e) textured and (f) planar surface.

It should be noted that passivation after metallization ($J_{0,Met}$) is not considered here, which will be done in the future with the goal to produce low contact resistivities while also maintaining an excellent passivation. It is expected that this is a main challenge when trying to move the FPC approach forward.

Summary

In conclusion, high iV_{OC} values of up to 719 mV and low contact resistivities down to 1 mΩcm² underline the potential of the FPC approach for APCVD (p) poly-Si layers. In general, higher firing temperatures produce lower ρ_C values. SEM images after polishing of the wafer cross-sections reveal a higher density of Ag crystallites within the poly-Si layer at higher temperatures, explaining this effect. A clear thickness dependence is visible where thicker layers lead to lower ρ_C values. This can be explained by a larger contact area of Ag crystallites to the poly-Si layer, thus decreasing the contact resistivity. Furthermore, multiple drive-throughs of the same wafer during deposition for thicker layers can also increase crystallinity and conductivity of the poly-Si, which then positively impacts the contact resistivity. Investigations regarding the passivation under the metal contacts ($J_{0,Met}$) should be done in the future to move forward the FPC approach with APCVD (p) poly-Si.

Data availability statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Author contributions

Competing interests

The authors declare no conflict of interest.

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