ULTRA-LARGE 20X20CM² MULTI-CRYSTALLINE SOLAR CELLS FIRST EXPERIMENTS AND LIMITS FOR INDUSTRIAL SOLAR CELL PRODUCTION

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ABSTRACT: Processing of solar cells on ultra-large scale multi-crystalline wafers (ULS) with 200 or 210mm edge length respectively are latest development of industry in Japan and Germany. The first modules with ULS solar cells are available in year 2005 and it seems a real trend of production technology comparable with decreasing wafer thickness. The reason for this development is the strong necessity of PV industry to reduce costs per W_{peak}. First experiments were carried out on ULS wafer material, in order to define the major problems and limits for industriallike production. The potential of cost reduction and limits of efficiency and yield were calculated. The difference of production lines with a batch-type production and inline-type production will be compared. A significant cost reduction can only be achieved with a batch-type production line, with yield and efficiency only slightly decreased.

Keywords: Manufacturing and processing - 1, multi-crystalline - 2, sizing - 3

1 INTRODUCTION

Thinner and larger wafers are two possible ways to decrease solar cell production costs without major changes of cell production technology. While reducing wafer thickness implies the risk of higher breakage rates and increased cell bending, processing of larger wafers is a definite trend of photovoltaic industry. 1980 industrial production of silicon solar cells still was mainly based on $100 \times 100 \text{ mm}^2$ silicon wafers.

Latest production facilities are able to process 6 inches mono- or multi-Silicon wafer material fully automated. But wafer sizes of up to 8 inches ($210 \times 210 \text{ mm}^2$) are already announced. Production start of these ultra-large scale wafers (ULS) in Germany will be 2005.



Figure 1: Development of cell size and area over the last years. A dramatic increase of wafer size during the last few years is obvious.

Figure 1 shows history and actual status of this enlargement in terms of size and single product area. This is a significant difference to chip production, where wafer size increases in a similar way, but single product area almost remained the same.

The enlargement of wafer size within the last 10 years by 100% implies an inherent advantage of wafer size for solar cell production. This is of course lower production costs per Wpeak due to higher production capacity, less handling steps per Wpeak (wafer, cell and module production) and higher packing density in the

module. Within this work only solar cell production was investigated.

2 WAFER STABILITY

Taking a closer look to the differences of processing ULS wafers compared to standard wafers, the main issue is more complicate handling and stability issues. The technological challenges of processing ULS wafers are:

- Mechanical yield during wafer manufacturing
- Mechanical yield in cell production line
- Accuracy of automation
- Homogeneity over total wafer surface (diffusion, SiN-deposition, screen-printing)

To estimate the mechanical yield, wafers of different size were tested with a stability testing tool. The system was used in a twist testing configuration, which gives a relatively good correlation with stress during processing. Figure 2 shows almost no stability change (measured was max. force or breakage force) for the range of wafer sizes. On the other hand absolute bending of wafers is increased and can cause handling problems.



Figure 2: Stability of wafers (breakage or max. force) is independent of wafer size. Maximum bending or bowing of ULS wafers is increased by a factor of 2 compared to 125mm wafers (thickness of all wafers $300\mu m \pm 30$).



Figure 3: Wafer resilience of ULS wafers are decreased dramatically.

First experiments on ULS wafers were carried out, showing a different aspect. In spite of the stability experiments wafer breakage was dramatically increased (appr. by a factor of 2) during wafer manufacturing and cell processing.

Possible reasons for this can be:

- low experience with ULS-wafers
- temperature inhomogeneities during firing
- non-adjusted screen-printing for ULS wafers

Figure 3 shows the decrease of resilience for ULS wafers, which is in the expected range for similar wafer thickness ($\sim 300 \mu$ m) and larger wafer area. Automation and handling has to be adjusted in order to fulfil the ULS requirements. The effect seems to be quite similar to that of thin wafer handling (150 – 200 μ m thickness).

3 DOES SIZE REALLY MATTER?

Yes, size does matter: Cost calculation in comparison with 125 and 156 mm sized cells show great cost reduction potential of ultra-large-scale (ULS) wafers.

No principle efficiency limitations are related to wafer enlargement. But in comparison with chip industry product size of solar cells is total wafer size and leads to additional problems during back-end production (automation & yield). Therefore new production equipment has to be developed e.g. tabbing or stringing machines to handle three busbars per cell.



Figure 4: Correlation of lower efficiency and estimated production costs per W_{peak} (details see table 1).

Furthermore a calculation about the influence on cell parameters of separate areas with worse wafer quality has to be carried out. It could be even cost effective to cut ULS cells to four separate cells to overcome this problem. This will be a topic to be analyzed with a high-throughput production line using ULS wafers.

First calculations and running production sites show: cost reduction can be achieved by wafer enlargement from 125 to 150 and 156 mm respectively (edge length) up to 10%. The main uncertainty right now is the wafer price for ULS wafers. But with growing market share, there should be no significant increase on wafer price per area. In our calculations for 156 mm wafers a cost increase per wafer area of 2.5% and for 210 mm wafers of 5% are assumed.

Enlargement of wafer size does of course not lead to further cost reduction, if yield or efficiency will be decreased at the same time. The influence of both aspects to cost reduction potential of ULS wafers was calculated as well. Figure 4 shows the estimated production costs of ULS wafers with different efficiency levels. As a standard value for 125mm wafers 2€ per Wpeak was set.

Table I: Cost calculation for wafer size increase in a batch-type production facility (costs are normalized to $2\notin/W_{peak}$ for 125mm wafer size). Calculations show effective cost reduction potential and 210mm production sites in Germany starting in 2005 will potentially proof this thesis:

Cell Size [mm] (edge length)	125	156	210
Area [cm ²]	156,25	243,36	441,00
Efficiency [%] (average)	14,8%	14,7%	14,5%
P _{mpp} [W] (average)	2,30	3,59	6,39
I _{SC} (mA/cm ² , average)	32,1	32,1	31,6
I _{SC} [A] (average)	5,02	7,81	13,92
Yield [%] (of production line)	97%	96%	95%
Cycle Time [sec] (Batch)	3,0	3,0	3,0
Investcost Increase (Batch)	0%	20%	40%
Cycle Time [sec] (In-line)	3,0	3,7	5,0
Investcost Increase (Inline)	0%	5%	10%
Capacity [pcs/hr] (per line, Batch type) *)	1200	1200	1200
Capacity [pcs/hr] (per line, In-line) **)	1200	962	714
Total Capacity [MW/yr] (Batch) ***)	18,5	28,6	50,5
Capacity Increase [%]	0%	55%	173%
Total Capacity [MW/yr] (In-Line) ***)	18,5	22,9	30,1
Capacity Increase [%]	0%	24%	62%
Batch-Type Production Costs [€ / W _{peak}]	2,00€	1,86€	1,70€
Cost Reduction	0%	-7%	-15%

") only edge length limitation

**) 300 working days / 23 hrs uptime per day

No cost reduction potential could be shown for inline production facilities due to reduced throughput. This is of course only valid for a single line with a decreased "cycling-time" corresponding to edge length of wafer.

Even for efficiencies of below 13% a cost reduction potential can be achieved, assuming that wafer costs per area are only slightly increased (by 5%).

Cost reduction potential for yield decrease is comparable to influence of efficiency. Even for yields well below 90% a cost reduction is feasible. These calculations show the cost reduction potential of ULS wafers in cell production. Assuming that all production and cell values are the same for ULS wafers compared with 125mm wafers a cost reduction of up to 20% can be achieved. Taking into account additional effects during module production, the potential value of wafer size enlargement compared to wafer thickness reduction becomes obvious. Further enlargement of wafer size seems to be limited mainly by handling problems and wafer production.



Figure 5: Correlation of lower mechanical yield and estimated production costs per W_{peak} (details see table 1).

First experiments were carried out in order to verify the assumptions taken for the shown calculations.

4 FIRST EXPERIMENTS WITH ULS WAFERS

Processing of 150mm edge length has been established as a standard processing size at University of Konstanz. First experiments on 200mm wafers were carried out with alternative emitter diffusion (spray-on technique). Process sequence of all other steps are comparable to standard screen printing process (saw damage etch, emitter diffusion, plasma etching for edge isolation, P-glass removal, PECVD SiN-deposition, screen-printing of front and rear side, co-firing). Processing of all steps has to be adapted to ULS wafer material.

Calculations based on existing results show, that front grid design optimum is a three bus bar design (figure 6). The efficiency results of these first experiments were rather low compared to an average of >15% on smaller wafer size, but increased significantly from one experiment to the other (figure 7).



Figure 6: Calculation of efficiency potential with different front grid designs (2, 3 and 4 busbars compared with 125mm standard cell). 2 bus bar cell shows lowest performance.



Figure 7: Results of first successive experiments show "learning curve" of processing and handling.

5 SUMMARY

Wafer size enlargement seems to be an effective cost reduction strategy of solar cell production. Several cell manufacturers already announced production of multicrystalline solar cells based on ULS wafer material.

Our calculations show, that a minimum of 12.3 % efficiency or on the other hand a minimum yield of 88% is needed to get a cost reduction compared to 125mm cells. Using the assumptions of table 1 only an increase of wafer price >24% would be the limit for a cost reduction potential. If all production values would be the same as for standard wafer size and cost of wafer area would be the same a cost reduction potential of around 20% can be assumed.

Running projects of industry will proof the ability to realise low prize cells and modules based on ULS wafers.

6 ACKNOWLEDGEMENTS

This work was partly supported within the CRYSTAL CLEAR program by the European Commission.

We would like to thank PV Silicon for delivery of ULS multi-crystalline wafers.