ULTRA-LARGE 20 X 20 CM^2 MC-SI SOLAR CELLS: IMPROVED CELL PROCESS RESULTING IN EFFICIENCIES EXCEEDING 15 %

Bernhard Herzog and Kristian Peter
University of Konstanz, Department of Physics, P.O.Box X916, D-78457 Konstanz, Germany
Phone (+49) 7531/88-2260, Fax (+49) 7531/88-3895, e-mail: bernhard.herzog@uni-konstanz.de

ABSTRACT: Wafer size enlargement seems to be an effective cost reduction strategy of solar cell production. Within the last 10 years wafer size in cell production increased from 10 x 10 cm^2 to 15.6 x 15.6 cm^2. The next step will be an enlargement of wafer sizes up to 8 inches. Some cell manufacturers already announced the production of mc solar cells based on ultra-large scale (ULS) wafers. But firstly technological challenges like mechanical yield during wafer and cell manufacturing respectively and homogeneity over total wafer surface have to be mastered (diffusion, texturisation, SiN-deposition, screen-printing). To be compatible to inline production lines cell processing experiments on ULS wafers were carried out using spray-on technique as alternative emitter diffusion. In the latest experiment we included a texturisation step in the process sequence resulting in a solar cell efficiency of 15.1 %.
Keywords: Sizing, Diffusion, mc-Si Solar Cells

1 INTRODUCTION

PV industry has to reduce costs per W_p if solar energy wants to become competitive to conventional energies. Thinner and larger wafers are two possible ways to decrease solar cell production costs without major changes of cell production technology. In the sixties industrial production of silicon solar cells in Germany started on 10 x 10 cm^2 silicon wafers. Latest production facilities are able to process 8 inches multi-crystalline silicon wafer material fully automated. The enlargement of wafer size within the last 10 years by 100% implies an inherent advantage of wafer size for solar cell production. This implicates of course lower production costs per W_p due to higher production capacity, less handling steps per W_p (wafer, cell and module production) and higher packing density in the module. Taking a closer look to the differences of processing ULS wafers compared to standard wafers, the main problems are a more complicated handling, stability and homogeneity issues.

2 COST REDUCTION POTENTIAL

Cost calculations in comparison with 12.5 and 15.6 cm sized cells were made showing a great cost reduction potential for ULS wafers in batch-type production lines [1]. Lower production costs per W_p can be achieved due to higher production capacity, less handling steps (wafer, cell and module production) and higher packing density in the module. No efficiency limitations are related to wafer enlargement in principle. But in comparison with chip industry product size of solar cells is total wafer size and leads to additional problems during back-end production (yield, automation and homogeneity over total wafer surface). Therefore new production equipment has to be developed, e.g. tabbing or stringing machines to handle three or four busbars per cell.

Assuming that all production and cell values are the same for ULS wafers compared to 12.5 cm wafers a cost reduction of up to 20 % can be achieved. Even for efficiencies of below 13 % and yields below 90 % (standard for 12.5 cm cells is about 97 %) a cost reduction is feasible.

But the actual trend in industry is towards thinner wafers (230 µm and thinner) as there is currently a lack of silicon feedstock on the market and production of thinner wafers leads to higher material yield. Therefore the cost savings for producing thinner cells are presently higher than for producing larger ones, because silicon feedstock and wafer material accordingly has become rather expensive. The minimum thickness of ULS wafers is limited mainly by stability and handling problems during cell and wafer production so that an application to very thin wafers is definitely difficult.

However, when the silicon feedstock bottleneck has overcome, the ULS wafer format might become more interesting for industry again.

3 EXPERIMENTS AND RESULTS

3.1 Improved cell process

Processing of 15.6 cm edge length has been established as a standard processing size at the University of Konstanz. Thus all process steps had to be adapted to ULS wafer material. As our diffusion tube furnace is limited to 15.6 cm wafer size, experiments on 20 cm wafers were carried out using the spray-on technique as an alternative emitter diffusion. Indeed this involved further effort in optimisation, but on the other hand the process is compatible to inline processing. Initially we integrated the spray-on diffusion into our standard solar cell process (saw damage etch, tube furnace $POCl_3$ diffusion, phosphorus glass etching, edge isolation, PECVD SiN_x ARC, screen printing metallization and co-firing) by replacing the $POCl_3$ emitter diffusion only.

For the precursor deposition we used a commercial available phosphorus spin-on dopant. The precursor was sprayed onto the wafer surface on both sides. Double sided diffused wafers have a better performance and higher open circuit voltage since phosphorus enables P-gettering of silicon during the diffusion process. After a drying step the diffusion was performed in a belt furnace at temperatures between 890°C and 920°C leading to sheet resistances of 30 to 50 Ω/sq. This cell process with spray-on diffusion provided ULS cells with acceptable performance and homogeneity resulting in efficiencies of about 15 % (40 Ω/sq emitter, 2 busbar front grid design, see Table II).

The latest experiment included a texturisation step in the process sequence (see Fig. 1). We used an acidic iso-texture, which was developed at the University of Konstanz. The texture was performed in a high-throughput inline system and replaces in our cell process the NaOH saw damage etch [2].

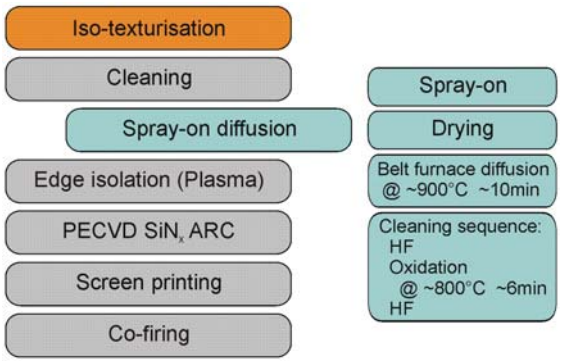

Figure 1: Flow chart of the improved solar cell process using iso-texturisation and spray-on diffusion technique

One major difficulty of the spray-on technique is the removal of dopant residuals on the wafer surface after the diffusion. For non-textured wafers a HF-dip followed by an oxidation at about 800°C in a belt furnace and a further HF-dip led to a clean and hydrophobic surface. As alternative cleaning step an acidic oxidation within a HF-Piranha etch-HF sequence is possible [3]. Even better and more suitable for industrial use would be a modified belt furnace design with additional oxygen supply. Diffusion, drive in and oxidation of the phosphorus glass could be achieved in one single step.

For textured wafers the removal of residuals turned out to be more difficult. The HF-oxidation-HF cleaning sequence resulted in partly hydrophobic wafer surfaces only. On some wafers remained residual spots leading to an inhomogeneous SiN_x deposition.

3.2 Cell results

Shown in Table I are the results for ULS cells with iso-texturisation. For the wafers of this experiment we chose a 40 Ω/sq emitter and a front grid design with two busbars.

Table I: Parameters of textured ULS cells with a 40 Ω/sq emitter and two busbar frontgrid design

	Bus-bars	Sheet res. [Ω/sq]	FF [%]	J_{sc} [mA/cm^2]	V_{oc} [mV]	η [%]
Best cell	2	39.6 ± 4	73.0	33.9	610	**15.1**
Mean (4 cells)	2	~ 40	73.1	33.7	610	**15.0**

In Table II are presented the results of the last experiment without texturisation step. Within this experiment as well a 40 Ω/sq emitter was used and most cells were processed with a two busbar frontgrid design, however a few cells were processed with four busbars.

Table II: Parameters of untextured ULS cells with a 40 Ω/sq emitter and frontgrid designs with two and four busbars respectively

	Bus-bars	Sheet res. [Ω/sq]	FF [%]	J_{sc} [mA/cm^2]	V_{oc} [mV]	η [%]
Best cell	2	40.7 ± 2	72.7	33.6	616	**15.0**
Mean (6 cells)	2	~ 40	72.3	33.5	617	**14.9**
Best cell	4	42.0 ± 2	75.0	32.7	617	**15.1**

The textured cells have a higher J_{sc} and fill factor, but a lower V_{oc} resulting in an efficiency of 15.1 % for the best cell (comparing only the two busbar cells). The gain in J_{sc} of only about 0.2 mA/cm^2 could be higher for textured cells. Reason for this rather low J_{sc} increase might be the inhomogeneous SiN_x deposition and losses due to an inhomogeneous emitter sheet resistance (best textured cell has a deviation of 4 Ω/sq compared to 2 Ω/sq for the best untextured cell).

The untextured cell with four busbars shows a higher fill factor due to lower series resistance losses in the front grid, but on the other side a lower J_{sc} due to increased shadowing.

The best textured ULS cell was cut into four separate 10 x 10 cm^2 cells in order to compare the cell parameters of big and small cells respectively. The results are shown in Table III.

Table III: Parameters of a textured ULS cell before and after cutting into four 10 x 10 cm^2 cells

	Bus-bars	FF [%]	J_{sc} [mA/cm^2]	V_{oc} [mV]	η [%]
ULS cell	2	73.0	33.9	610	**15.1**
Small cell 1	1	73.0	34.0	612	**15.2**
Small cell 2	1	73.3	34.0	614	**15.3**
Small cell 3	1	73.7	33.9	619	**15.4**
Small cell 4	1	74.3	33.9	616	**15.5**
Mean	1	73.6	34.0	615	**15.4**

The small cells show a much better performance than their ULS mother cell. This is mainly caused by lower series resistance losses as the ULS cell has to deal with a current of 13.5 A compared to 3.4 A for the small cells. Besides, the 100 cm^2 cells are quite homogeneous. This proves, that processing over the whole wafer area was acceptable homogeneous.

The results of the ULS cells were compared with a standard 12.5 x 12.5 cm^2 cell with iso-texturisation and $POCl_3$-emitter. The parameters of this reference-cell with two busbar frontgrid design are shown in Table IV. Apart from the diffusion step the 12.5 cm cell has the same process sequence as the textured ULS cells.

Table IV: Parameters of a textured 12.5 x 12.5 cm^2 cell with $POCl_3$-emitter

	Sheet res. [Ω/sq]	FF [%]	J_{sc} [mA/cm^2]	V_{oc} [mV]	η [%]
12.5 cm $POCl_3$	50 ± 1.4	76.6	33.0	617	**15.6**

We made LBIC maps of an untextured and a textured ULS and 12.5 cm reference cell respectively in order to check the process homogeneity over total wafer area. For the measurements a laser with a wavelength of 980 nm was used. The LBIC maps of the untextured ULS cell (with 4 busbars) and untextured reference cell are shown In Figure 2.

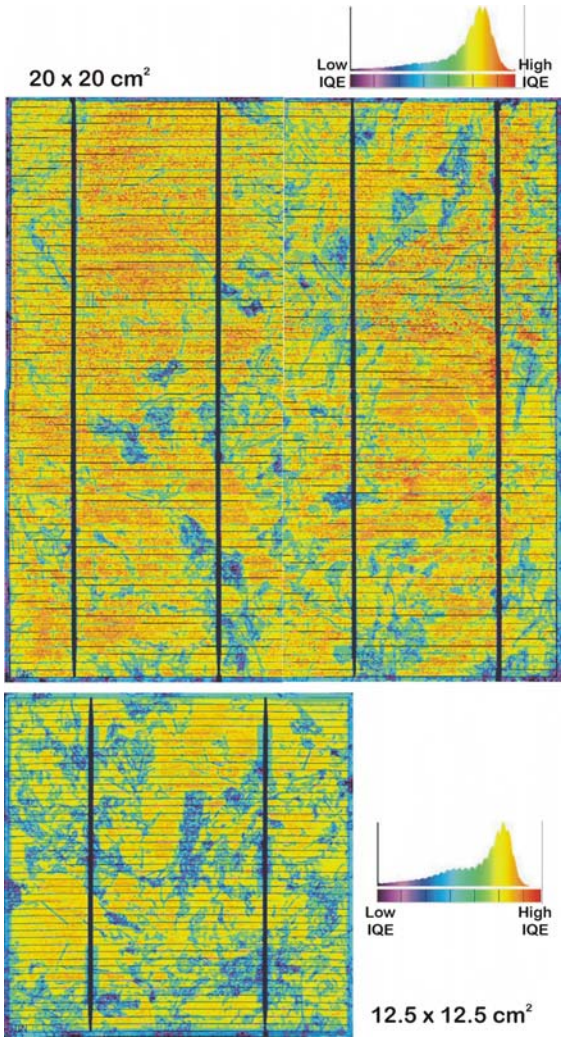

Figure 2: LBIC maps of an untextured ULS and reference cell

The IQE distribution is homogeneous for both the ULS cell and the reference cell.

Figure 3 shows parts of the LBIC maps of a textured ULS cell (with two busbars) and a textured reference cell.

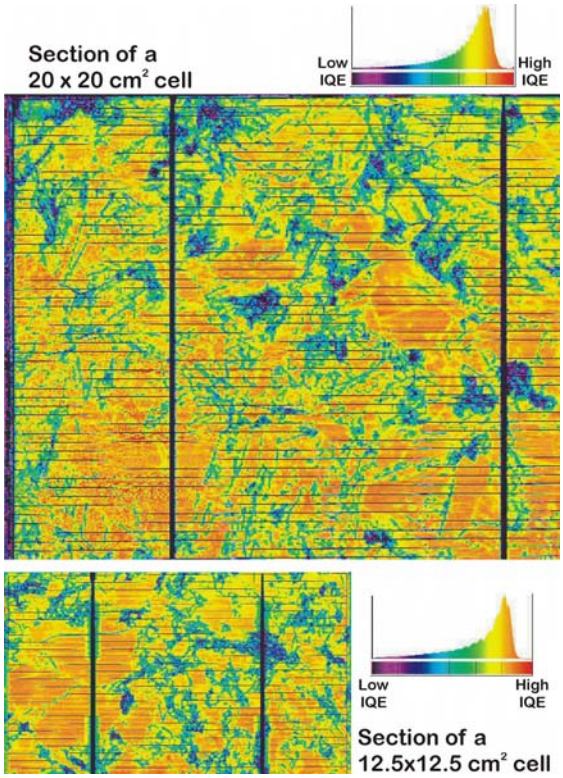

Figure 3: Parts of the LBIC maps of a textured ULS and reference cell

Again the IQE distributions over total wafer area of ULS and 12.5 cm reference cell are comparable homogeneous. This demonstrates again, that our cell process with texturisation is acceptable homogeneous.

In Figure 4 parts of the IV-characteristic of a textured ULS cell with two busbars, an untextured ULS cell with four busbars, a quarter of a textured ULS cell (one busbar) and of the textured 12.5 cm reference cell are shown.

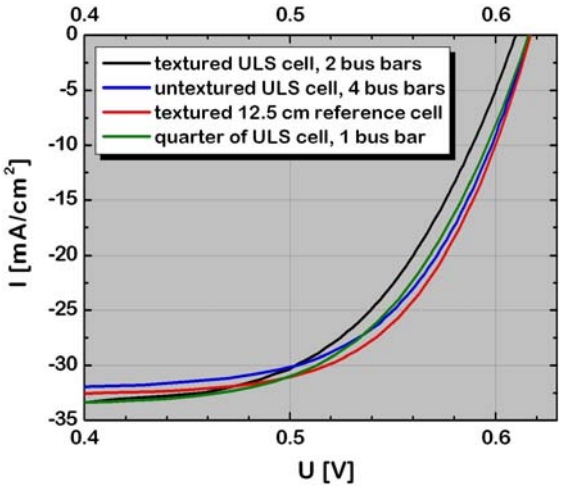

Figure 4: Parts of the IV-characteristic of ULS and reference cells

In the region between 0.55 V and 0.62 V the 12.5 cm cell shows the highest slope and the textured ULS cell with two busbars the lowest one. This is due to higher series

resistance losses in the front grid. The IV-characteristics were fitted with the 2-diode-model. The results for the series resistance are presented in Table V.

Table V: Series resistance data of ULS and reference cells fitted with the 2-diode-model

	Textured ULS (2BB)	Untextured ULS (4BB)	Textured 12.5 cm	Quarter ULS (1BB)
R_{series} [Ωcm^2]	1.15	0.85	0.69	1.01

As expected from Figure 4 the textured 12.5 cm reference cell has the lowest series resistance, followed by the untextured ULS cell with four busbars. The quarter ULS cell with one busbar and the complete ULS cell with two busbars have the highest series resistance.

Spectral response measurements show that the reflection of the textured ULS cell at lower wavelengths is higher than the one of the 12.5 cm reference cell (see Fig. 5). Moreover the textured ULS cell has a worse IQE in the emitter region. This proves that texturisation, spray-on diffusion, cleaning after diffusion and SiN_x deposition are not perfectly adjusted. Optimisation of these process steps will be part of the next experiment.

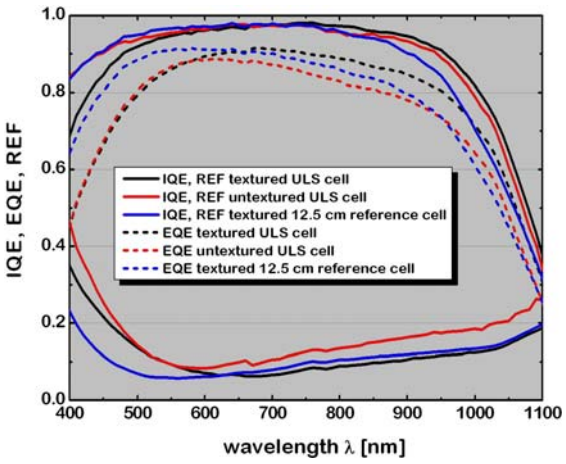

Figure 5: Spectral response measurements of a textured ULS cell, an untextured ULS cell and a 12.5 cm reference cell

4 CONCLUSIONS

In principle there is a great cost reduction potential for ULS wafers in batch-type production lines. But actually silicon feedstock and wafer material has become so expensive, that presently the cost savings for producing thinner cells are higher than for producing larger ones. But this situation could change when in some years the silicon feedstock bottleneck has overcome.

Our experiments on ULS wafers were carried out using the spray-on technique as alternative emitter diffusion. We integrated a texturisation step in the process sequence. Both for textured and for untextured cells we reached efficiencies of 15.1 % (on different front grid designs). We have shown that our solar cell process for textured and for untextured cells is acceptable homogeneous, but there is still potential for optimisation.

5 ACKNOWLEDGEMENTS

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