10 x 10 cm^2 SCREEN PRINTED BACK CONTACT CELL WITH A SELECTIVE EMITTER

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ABSTRACT

Back contact cells promise a cost reduction for the interconnection of cells to modules. The Emitter Wrap Through concept allows in addition to combine low cost material, surface texture, a selective emitter (alkaline etch for Cz-Si respectively mechanical texturing for mc-Si) together with screen printed contacts as done in this work. The connecting holes are drilled by a laser. Emitter and base region at the cell rear are separated by a screen printable diffusion barrier. Computer simulations assisted the optimisation of the grid design especially in estimating the influence of the busbar regions to the series resistance. An efficiency of 15.8 % was reached on Cz-silicon, which is the highest efficiency reported so far for a low-cost (i. e. no photolitographical steps) back contact cell. We obtained J_{sc} of 37.9 mA/cm^2 and V_{oc} of 600 mV. The internal quantum efficiency was found to be distinctly increased due to the selective emitter on the front.

INTRODUCTION

Back contact cells promise a cost reduction for the interconnection of cells to modules [1]. The Emitter Wrap Through concept allows in addition to combine low-cost material, a selective emitter and screen printed contacts [2,3]. The front side emitter is connected through small laser drilled holes to the rear emitter contact (Fig. 1). The short circuit current is distinctly increased due to the second carrier collection junction at the cell rear as well as by avoiding grid shadowing losses [4].

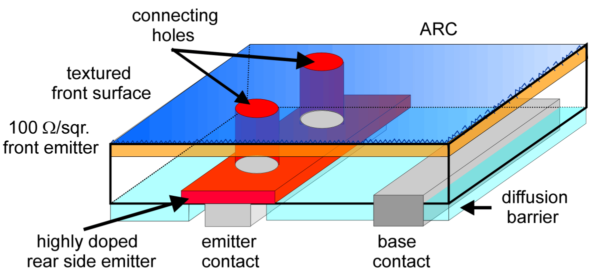

Fig. 1. Sketch of a low cost back contact cell. Emitter and base region at the cell rear are separated by a diffusion barrier. Small laser drilled holes connect front and rear side emitter.

The appealing uniform front view makes this cell concept especially suitable for facade and similar applications where a pleasant appearance is demanded. The most crucial point in back contact cells is the separation of the p- and n^+-area at the cell rear. Several methods have been investigated in the past [2,4,5]. They can be divided into two groups: either the n^+- layer is removed after diffusion (e. g. by mechanical or laser abrasion [4]) or the diffusion at the later p-region is prevented by a diffusion barrier. In addition, the use of silicon nitride or oxide as diffusion barrier passivates the pn-junction at the surface which is very important to obtain a satisfying open circuit voltage [6]. Both, oxide as well as nitride are applied over the hole rear area and have to be locally removed using some sort of masking pattern (e.g. photolithography [7,8,14], screen printable etch masks [9,10], etc.). This procedure is quite time consuming and does not seem to be really compatible to the low-cost approach of the cell concept. So investigations on a screen printable diffusion barrier have been undertaken and are presented in the following.

PROCESS

The production process is briefly described: the front surface is textured for improved optical confinement. This can be done by alkaline texture etch in the case of Cz-silicon or by a mechanical structuring tool for multicrystalline silicon. A $POCl_3$- diffusion with a sheet resistance of around 100 Ω/sqr follows. The frontside is then protected by a LPCVD Si-nitride. Texture etch, high-ohmic emitter diffusion and LPCVD-SiN deposition were performed by BP Solar. The connecting holes are drilled by a Nd-YAG-laser which is a flexible tool for experimental studies and which could also be applied in an industrial environment [1]. Holes are conically shaped which is favourable for the series resistance.

After alkaline damage etch a diffusion barrier is locally screen printed on the rear side in order to separate the interdigitated emitter and base region at the cell rear. Drying and curing of the barrier paste follows. Wafers are cleaned in diluted HF. A second $POCl_3$ -diffusion comes next generating a sheet resistance of around 10 Ω/sqr to ensure a high conductivity inside the holes as well as a low contact resistance to the screen printed contacts. P-glass is removed in diluted HF. Emitter and base contacts are screen printed using an automatic alignment system and co-fired in an IR-belt furnace (Fig. 2). The connecting holes are partially filled with silver paste to keep the series resistance low. Notice, that no kind of edge isolation is necessary.

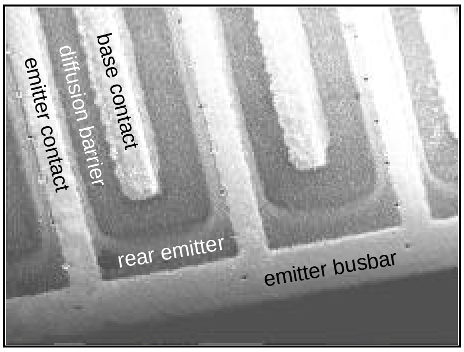

Fig. 2. SEM-picture of the rear side of a screen printed back contact cell with printed diffusion barrier. The small connecting holes are drilled by a laser.

GRID OPTIMISATION

A large number of investigations has been undertaken to optimise the rear grid design. In conventional cells the optimum between resistance and shadowing losses determines the grid design. In back contact cells the optimum is more difficult to determine. A compromise between alignment accuracy, contact resistance and collection enhancement due to the rear emitter has to be found. Multiple and wide busbars decrease the series resistance in the metallization, but increase the series resistance inside the silicon by an extended path to the neighbouring finger contact (Fig. 3). Computer simulations (DESSIS$_{TM}$) can assist these optimisation as they allow to evaluate the effects of the different grid parameters, however optimising a complete back contact cell with its highly 3-dimensional structure only by computer simulations is not possible with our means.

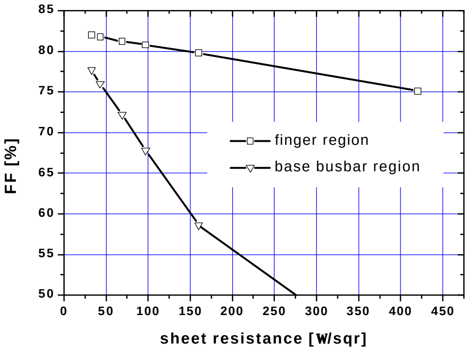

Fig. 3. For a given busbar width the FF in dependence on the front emitter sheet resistance was simulated with DESSIS$_{TM}$. As a result the area covered by the base busbars should be minimised.

The sheet resistance of the front emitter has also been optimised by numerical studies: current gain and increased series resistance have been compared (Fig. 4). The two base busbars with only 6.4 % of the whole cell area, reduce the fill factor already by about 3 % (absolute).

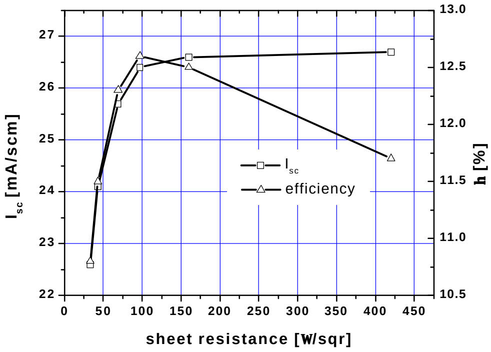

Fig. 4. In the simulation short circuit current and cell efficiency show an optimum at a front emitter sheet resistance of around 100 Ω/sqr (no ARC). Further increase of the sheet resistance increases R$_{serie}$, but contributes little to increase J$_{SC}$.

DIFFUSION BARRIER

Several screen printable pastes of different suppliers have been investigated. As the application of a diffusion barrier is rather uncommon for the PV-industry information about pastes, properties and curing temperatures were hard or even not at all to be optained. Best results have been reached with a commercially available paste developed for a different application. The curing temperature for optimum blocking properties was found to be in the range of 1000 °C.

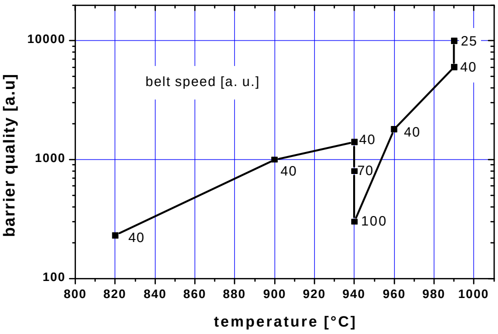

Fig. 5. Blocking quality of the barrier paste depending on the curing temperature and time. The small numbers next to the data points indicate the belt speed. The blocking quality was measured as ohmic resistance between screen printed contact pads. Hot is favourable to obtain an efficient diffusion barrier.

Once the fire parameters are determined, the paste can be normally processed. Line broadening is in an acceptable range. After curing the colour of the layer appears dark blue, which simplifies the alignment in combination with the automatic alignment system.

Problems with low values of the shunt resistance are often reported in back contact cells [1,2,9,11]. Shunt values of the cells with screen printed diffusion barrier investigated in this work are between 1000 and 2000 Ωcm^2 which is even higher than for cells using Si nitride as diffusion barrier. Above 1000 Ωcm^2 the negative effect on the cell performance is negligible.

RESULTS

An efficiency of 16.1 % was reached on 10 x 10 cm^2 Cz-silicon, J_{sc} of 37.9 mA/cm^2 and V_{oc} of 600 mV with a single ARC of LPCVD Si-nitride. V_{oc} is slightly lowered compared to conventional cells due to the additional dark current of the rear emitter area [4]. The series resistance is increased due to the base busbar regions and due to the base *grid* metallisation instead of a fully metallized rear side. Also the current path inside the holes contributes to R_{serie}. A selective emitter (highly doped inside the holes) reduces this contribution as well as a larger hole diameter (the latter interferes with the optical requirements of a uniformly appearing front side, Fig. 7). The series resistance is the most limiting condition for the fill factor. Using a model of distributed series resistances [12] values between 1 Ωcm^2 and 2.5 Ωcm^2 have been fitted. These rather high values are responsible for the moderate fill factors of around 70 %.

Table 1. IV-results for different front emitter treatments (Cz-silicon unless otherwise indicated). A comparison of SiN and a screen printable paste as diffusion barrier is also shown. The fill factor is mainly limited by R_{serie}. Several different causes due to the EWT-design contribute to R_{serie}. V_{oc} of the mc-cell can very probably be increased by hydrogen passivation.

	J_{sc} [mA/cm^2]	**V_{oc} [mV]**	**FF [%]**	**h [%]**	**R_{serie} [Wcm^2]**
homog.	34	586	66	13.1	2.1
hom/text	36.2	594	64	13.8	2.0
select/textured/ SiN as barrier	37.8	599	72	16.1	1.3
select/textured/ barrier paste	37.9	600	70	15.8*	1.5
multicrystalline Si, mech. text., select. emitter	35.8	571	65	13.2	1.7
conv. cell	31.7	621	77	15.1	0.4

* independently confirmed at JRC, Ispra, Italy

The increase of J_{sc} compared to a conventional cell splits in 3 parts: Avoided shadowing losses increase J_{sc} by about 8 %. The rear emitter increases J_{sc} by about 4 %. Simulations indicate another increase of 12 - 15 % due to the selective emitter which however is smaller in the experiment but can be reached combined with the microtexture. The selective emitter improves the IQE distinctly in the short wavelength range (Fig. 6), the effect of the rear side emitter on the IQE is less obvious. However, in an LBIC scan the rear side structure is very well visible and shows a difference in the collection probability of around 15 % between emitter and base area at 905 nm [13].

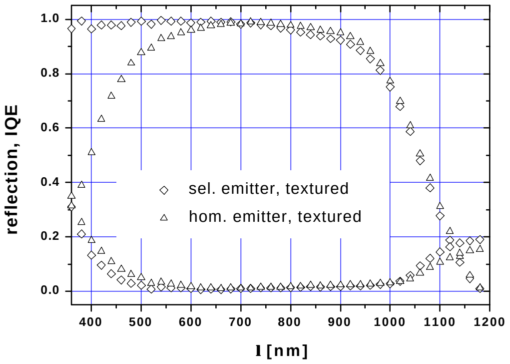

Fig. 6. Internal quantum efficiency of an EWT-cell with selective emitter compared to an EWT-cell with homogenous emitter, both Cz-silicon. The selective emitter increases J_{sc} from 36.2 mA/cm^2 to 37.8 mA/cm^2.

Analysing the IQE with IQE-1D™ leads to a surface recombination velocity of 2100 cm/s for the selective emitter, compared to more than 4*10^5 cm/s for a homogeneous 35 Ω/sqr emitter. The base diffusion length is about 220 µm. For better comparison this investigation was done on Cz-silicon. The weighted rest reflection is 4 %, in contrast to around 10 % for an untextured EWT-cell and about 19 % for a conventionally processed cell.

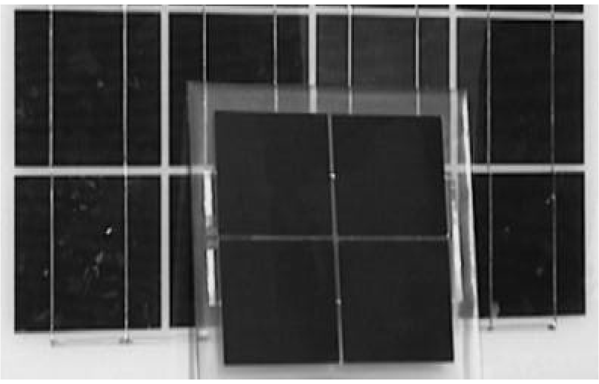

Fig. 7. Photo of a mini-module made of 4 back-contact cells (Cz) in front of a module of conventional cells. The back-contact cells can be arranged with nearly no space between them. The homogeneous optical appearance is very appealing compared to the conventional cells with the reflecting busbars. The mini-module was IV-measured at ECN, Netherlands, with J_{sc} = 3.62 A, V_{oc} = 2.39 V and an efficiency of 14.0 %.

CONCLUSION

A low cost back contact silicon solar cell was presented. Front and rear emitter are connected by small laser drilled holes. Emitter and base area at the cell rear are separated by a screen printable diffusion barrier. Contacts are screen printed using an automatic optical alignment system. The front emitter is a highquality selective emitter. Due to the EWT-concept no further alignment steps are necessary for the selective emitter. The efficiency of the cell is limited by the moderate fill factor which is affected by the relatively high series resistance (associated with cell concept). 15.8 % confirmed cell efficiency have been reached with this process (16.1 % using SiN as diffusion barrier). This is to our knowledge the highest efficiency reported for a low cost (no photolithography) screen printed back contact cell.

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REFERENCES

[1] J. M. Gee, W. Schubert, and P. Basore, ”Emitter Wrap-Through Solar Cell“, *Proc. 23th IEEE PVSC*, 1993, p. 265

[2] A. Schönecker, A. Weeber, W. Sinke, C. Zechner, A. Kress, and P. Fath, ”Attacking limiting factors in 10 * 10 cm^2 multicrystalline silicon, Emitter Wrap-Through solar cell design and processing“, *Proc. 2nd WCPSEC*, 1998, p. 1677

[3] A. Kress, P. Fath, and E. Bucher, ”Recent results in low cost back contact solar cells“, *Proc. 16th EPSEC*, 2000, in print

[4] A. Kress, P. Fath, G. Willeke, and E. Bucher, ”Low-Cost back contact silicon solar cells applying the Emitter-Wrap Through (EWT) concept*“, Proc. 2nd WCPSEC*, 1998, p. 1547

[5] A. Kress, R. Kühn, P. Fath, and E. Bucher, ”Low-cost back contact silicon solar cells“, *IEEE transactions on electron devices* **46** (10), 1999, p. 2000

[6] R. Kühn, A. Boueke, M. Wibral, C. Zechner, P. Fath, G. Willeke, and E. Bucher, ”Investigation of the effect of p/n-junctions bordering on the surface of silicon solar cells“, *Proc. 2nd WCPSEC*, 1998, p. 1390

[7] D. D. Smith, and J. M. Gee, ”Review of back contact silicon solar cells for low-cost application“, *Proc. 16th EPSEC*, 2000, in print

[8] S. Hamamoto, H. Morikawa, H. Nwomoto, Y. Kawama, A. Takami, S. Arimoto, T. Ishihara, and K. Namba, ”Development of the VEST cell process for low-cost fabrication“, *Proc. 14th EPSEC*, 1997, p. 2328

[9] A. Kress, P. Fath, G. Willeke, and E. Bucher, ”Low-cost back contact silicon solar cells“, *Proc. 11th PVSEC*, 1999, p. 919

[10] A. Schönecker, H. H. C. de Moor, A. Burgers, A. Weeber, J. Hoornstra, W. Sinke, P.-P. Michiels, and R. A. Steeman, ”An industrial multicrystalline EWT-solar cell with screen printed metallisation“, *Proc. 14th EPSEC*, 1997, p. 796

[11] A. Kress, O. Breitenstein, S. Glunz, P. Fath, G. Willeke, and E. Bucher, ”Investigations on low-cost back contact silicon solar cells“, *Solar Energy Materials & Solar Cells*, 2000, in print

[12] B. Fischer, P. Fath, and E. Bucher, ”Evaluation of solar cell J(V)-measurements with a distributed series resistance model“, *Proc. 16th EPSEC*, 2000, in print

[13] A. Kress, T. Pernau, P. Fath, and E. Bucher, ”LBIC measurements on low-cost back contact solar cells“, *Proc. 16th EPSEC*, 2000, in print

[14] S. W. Glunz, J. Knobloch, C. Hebling, and W. Wettling, "The range of high-efficiency silicon solar cells fabricated at Fraunhofer ISE", *Proc. 26th IEEE PVSC*, 1997, p. 231