COMPARISON OF DIFFERENT TECHNIQUES FOR EDGE ISOLATION

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ABSTRACT: In most industrial type solar cell processes the edge isolation is an important step. After most emitter diffusion techniques, especially the $POCl_3$ diffusion, the front contact is connected with the back contact through the emitter around the edge of the solar cell. As a common technique in industry this shunt is removed by plasma etching of the wafer stack. Other techniques which were investigated are: the grinding of the wafer edge with sandpaper, the cutting of isolation trenches with a wafer dicing saw and the laser separation by inserting trenches, the latter two techniques applied on both sides of the wafer. All these technologies are compared concerning their impact on the solar cell performance of industrial type screen printed solar cells. Using IV measurement (illuminated and dark), laser beam induce current (LBIC) and lock-in thermography it is shown that isolation by laser still suffers from too low fill factors and sawing, grinding, or plasma etching are preferable. A good correlation between decreasing shunt resistance and increasing amount of detected shunts using in-lock thermography or LBIC is found.
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1. MOTIVATION

A very simple but important step in most solar cell processes is the edge isolation. There are several approaches to avoid this step (co-diffusion [1], diffusion barriers by means of printing [2] or silicon nitride (SiN), one-sided emitter, ...) but most solar cells still have to be isolated. In industry the plasma etching of wafer stacks is very common, but this step is not in-line capable and undesired chemicals have to be used. Therefore there is a demand for other possibilities, which can be performed in-line, are easy to implement and cheap to realize. Besides the physical ability of each technique to remove the shunts also the advantages and disadvantages for an industrial usage are for interest.

2. DIFFERENT TECHNIQUES FOR ISOLATION

In addition to plasma etching 3 other techniques were used, which are further subdivided in 2 variations. This leads to the following 7 techniques:

1. Laser on the front side
2. Laser on the back side
3. Sawing trenches in the front side
4. Sawing trenches in the back side before/after printing
5. Grinding with sandpaper
6. Grinding with a beltsander
7. Plasma etching

Considering the demands of the industry using to insert trenches (Fig. 1) is the smartest way to remove the shunts, because it is contactless, fast, easy to align and no chemicals or susceptible mechanics are needed. But the fill factors reached on industrial type screen printed cells so far are too low. In this investigation the laser parameters of a Q-switched Nd:YAG laser were optimised, but with the used equipment (laser without optical scanning, slow tables) it was not possible to reach industrial relevant process times of some sec/wafer. In later experiments with industrial lasers the demanded time has been reached, but the results were not as good as in this investigation.

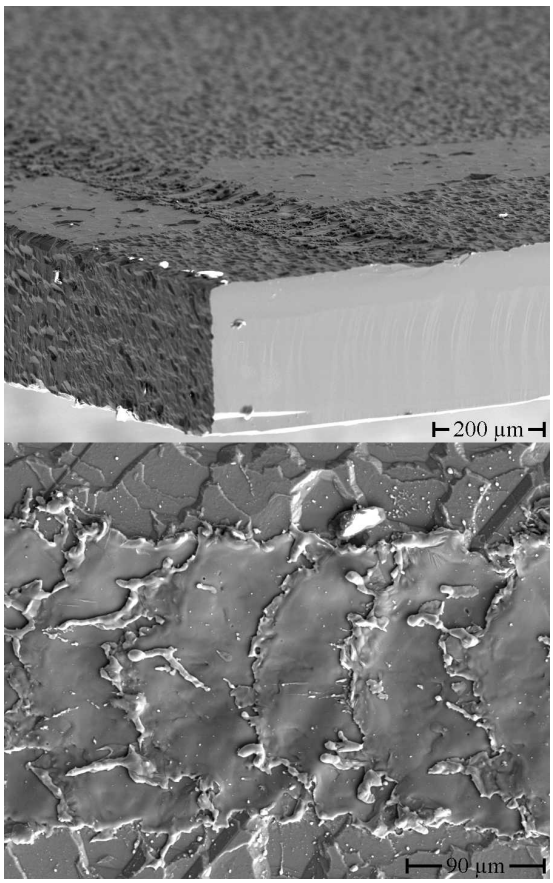

Figure 1: Electron microscope pictures of a laser trench. On the lower picture the trench is seen from top. The recrystallized structures of the laser spots can be seen. Laser was moving from left to right.

Sawing trenches in the wafer is a very common technique on the laboratory scale because it is easy to carry out and often the wafer has to be cut to a certain size anyway. Mostly trenches are cut and then the edge is broken off at this line, but in this case the edges were not broken. The trenches were cut in the front or back side respectively. Due to the shape of normal mc-Si wafers, which are not exactly square, the trenches have to be sawn at a certain distance from the edge in order to assure an overlap at the corners. This results in a loss of active area when sawing in the front side. As this feature was not optimised only the active area of each solar cell was considered in the IV measurement.

Grinding the edge of the wafer is a very easy and cheap way to remove the shunt. In this study this has been done by moving a small stack of cells back and forward on a piece of sandpaper or by pressing the cell stack on a commercial beltsander which is set up upside down. An industrial set-up wouldn't be very expensive, but the yield and throughput of such a machine had to be checked.

As already mentioned plasma etching is a very common method. In this case the etching was done after the plasma enhanced chemical vapour deposition (PECVD) SiN step. This lead to a certain removal of the SiN at the wafer's edge and therefore to an increased reflection in this area. Normally the plasma etching is carried out directly after emitter diffusion to avoid this effect.

3. EXPERIMENTS

A batch of 100 neighbouring mc Si wafers (10x10 cm²) was processed using the standard industrial type sequence at University of Konstanz (UKN): after a saw damage removal in NaOH the wafers were cleaned in HCl and HF subsequently. The following $POCl_3$ diffusion led to a 40 Ω/sq emitter. After removing the phosphorous glass the PECVD-SiN deposition was carried out. Then the wafers were printed using silver paste for the front side and aluminium paste for the back side and subsequently fired in an infrared furnace. When the edge isolation was carried out can be seen in Fig. 2.

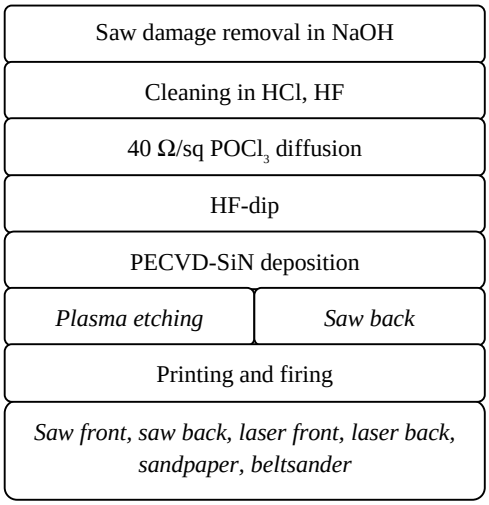

Figure 2: Processing sequence of the solar cells. The edge isolation steps are written in italics.

Half of the wafers for sawing trenches in the back side were cut before the printing and firing to see a possible influence of the firing step. It would also be more practical to do this before the firing, because in case of a back surface field created with aluminium paste there is a bending of the wafer, which makes it more difficult to fix the wafer with a vacuum on a chuck.

Then the solar cells were IV measured (illuminated, dark and I_{sc}-V_{oc}). The I_{sc}-V_{oc} curves were fitted with the 2 diode model setting the series resistance to zero. The obtained values for R_{sh} are too low, but they are comparable among each other and it is a fast method to characterise 100 solar cells. In addition J_{02} was evaluated to observe a damage of the space charge region. One typical cell of each group was fitted with all 3 IV-curves and LBIC measurements were carried out. In addition to a mapping of the whole wafer an area of 50x3 mm² at the edge of the corresponding wafers was measured with high resolution (25 µm). Finally these cells were mapped with lock-in thermography using an infrared camera at the Max Planck Institute of Microstructure Physics, Halle, Germany (MPI) for shunt detection [3].

4. SOLAR CELL RESULTS

The results of the solar cells with the different edge isolation methods used are presented in Fig. 1. The graph is divided in a lower part, where the mean values of efficiency Eta and fillfactor FF are shown and an upper part, where shunt resistance R_{sh} and saturation current density J_{02} are given. In this way all relevant physical parameters can be compared.

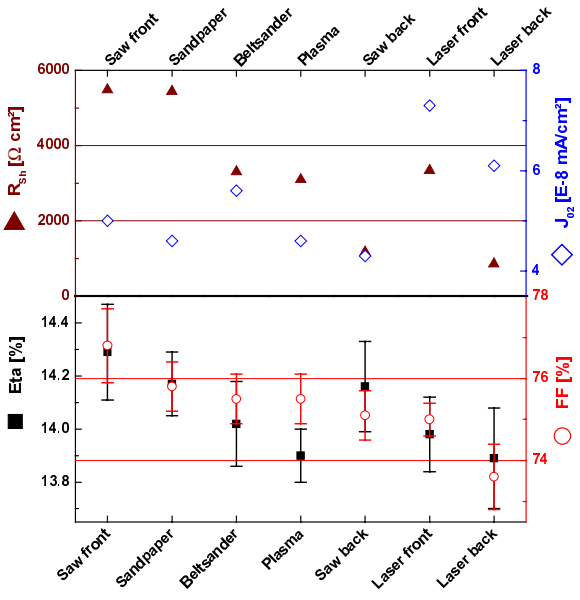

Figure 3: Mean values and deviation of Eta, FF, R_{sh} and J_{02}. There is a good correspondence between Eta and FF because V_{oc} was nearly identical and J_{sc} only differs due to increased reflection or improved collection ability (see text). The discrepancy between FF and R_{sh} can be explained with J_{02}.

The reached efficiencies of about 14 % are a little low, but we used a low quality material with an effective

minority carrier lifetime of less than 2 µs (as cut, without surface passivation). In addition the finished solar cells have not been tabbed, nevertheless the obtained fillfactors of up to 78 % are considerable high. This is very important because on this high level the differences caused by the different quality of edge isolation are better to distinguish.

The open circuit voltage V_{oc} is slightly influenced by the isolation method due to the differences in J_{02}, but the effect is very small, varying from 610 mV after using a laser to 612 mV isolated by a saw. The reached short circuit current density J_{sc} amounts to approximately 30.5 mA/cm² with 1 % higher values when isolating from the backside due to an improved collecting ability at the edges of the wafer (see Fig. 7) and with a little lower values using laser and plasma etching.

The mean values of the efficiency correlate to a great extent with the fillfactor. In case of plasma etching the SiN has been etched away on streaks up to 2 mm width from the edge of the wafer, which resulted in a higher reflectivity on these affected areas and therefore in a lower short circuit current density J_{sc}. This explains the gap between an average fillfactor and the worst efficiency. If the etching step had been carried out before the Sin deposition as it is normal this could have been avoided.

In case of the isolation methods on the back side of the wafer the efficiency is better than expected from the value of the fillfactor. Using these techniques the front side emitter is not affected at all and there is an increased carrier collecting ability due to the emitter going around the edge of the wafer connected with the front side. This can be seen in the LBIC map (Fig. 6). Both methods (laser and saw) applied on the back side suffer from a very low shunt resistance < 1000 Ωcm². This was also seen in [4]. In former experiments the sawing of trenches in the back side worked well, but this was not reproducible. In this case the low values are in agreement with LBIC and thermography measurements which will be discussed later. Sawing in the back side is still better than laser due to a little better R_{sh} but mostly due to a much lower J_{02}. This comparison is also valid using these techniques on the front side, but on a higher quality level. Again sawing results in a better isolation, but the greater effect is the difference in J_{02}. After laser treatment the saturation current is more than twice the value than after sawing.

5. LBIC AND THERMOGRAPHY

The LBIC measurements were carried out at UKN. Each of the 8 wafers was completely mapped with a resolution of 200-300 µm. In addition the same edge of each wafer was mapped on an area of 50x3 mm² with a higher resolution of 25 µm. The same wafers were then measured at the MPI using a lock-in thermography camera with a resolution of about 350 µm, a lock-in frequency of 13 Hz and a measurement time of 30 min/wafer.

What is obvious at first sight is the good correlation between shunt resistance and detected shunts on the wafers (Fig. 4). The mappings are arranged in the order of decreasing shunt resistance. Sawing trenches in the front side of the wafer resulted in the best shunt resistance of 10000 Ωcm² and no shunts at all are visible at the edge of the wafer. Within the wafer there are a few bright spots as on every measured wafer. Going to the last wafer, which has been sawn on the back side after the printing, the affected area with shunts is continuously increasing while the shunt resistance is decreasing to 900 Ωcm².

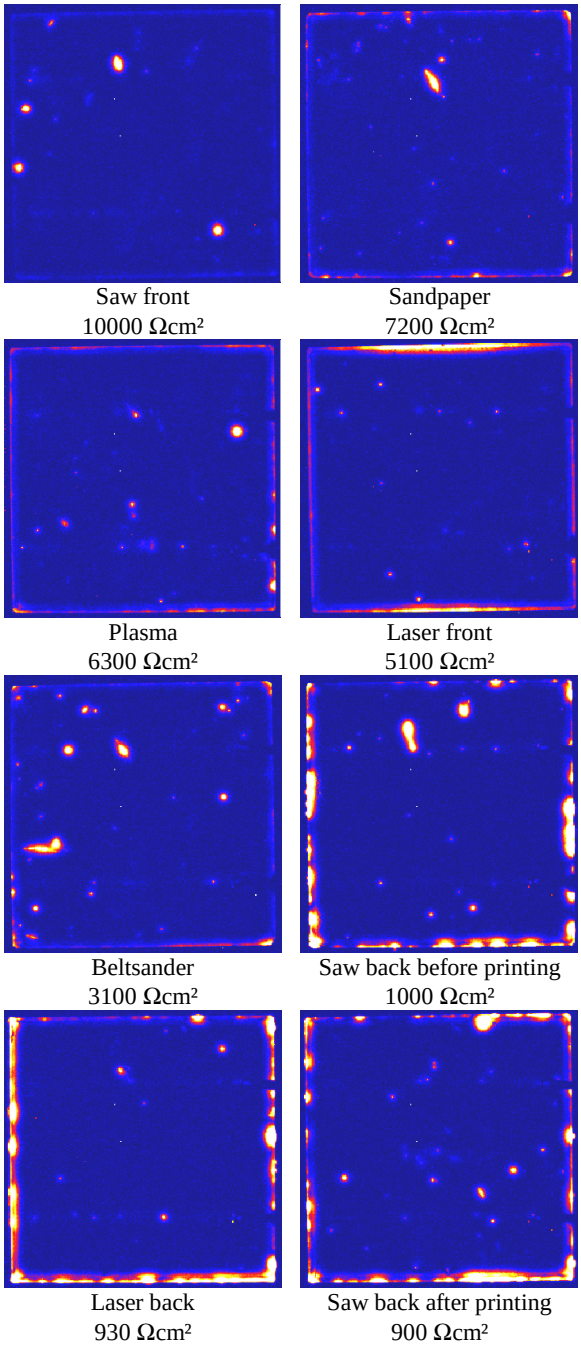

Figure 4: Lock-in thermograms of the solar cells with different edge isolation methods and fitted shunt resistance. There is a continuos increase of detected shunts (bright areas) with decreasing shunt resistance. In case of isolation on the back side the shunts are more pronounced and statistically distributed.

The thermogram of the wafer lasered on the front side shows an interesting effect on the horizontal edges. The extent of the shunt increases from the corners to the middle of the edge. As all wafers with an Al print for building a back surface field they show a bow after firing. This bow is in the direction of the described edges and therefore the laser is partly out of focus in the middle of the wafer. This defocusing is sufficient to decrease the energy density to an extent, that the evaporation of the silicon is limited. Probably a conducting layer is recrystallizing at the walls

of the lasered trench. This would explain the symmetric appearance of the detected shunt.

In contrast to this the shunts on the other wafers look more like spots or stains which are statistically distributed. This indicates that the shunt mechanism is in contrast to the effect during lasering on front not a systematical one.

A possible explanation could be that small cracks or damage created during cell process at the edge of the wafer is shunting the emitter with the p-doped base. When isolating the wafer on the back side these shunts still are connected with the front side emitter. Only by isolating on the front side or removing these areas by grinding or plasma etching the shunts are separated from the front side. First experiments to check this are in preparation.

On the LBIC maps of the whole wafers measured with low resolution it is very difficult correlate the local bad areas with the shunts detected by thermograms. This changes by mapping one edge of each wafer using a higher resolution. In this case some regions of the LBIC map can be identified without doubt as shunts (Fig. 5 & 6).

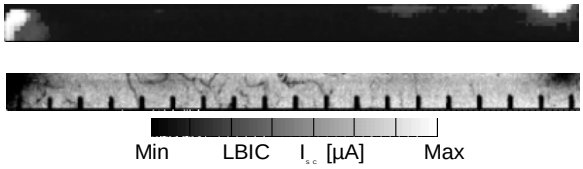

Figure 5: Magnified part of thermogram (top) and high resolution LBIC map (635 nm) (bottom) of the wafer isolated by laser in the back side. The two shunts can clearly be identified on both pictures.

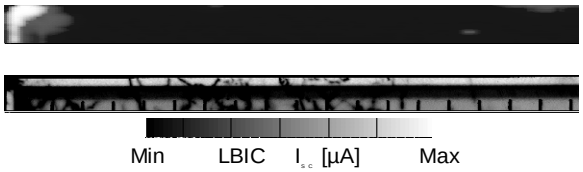

Figure 6: Magnified part of thermogram (top) and high resolution LBIC map (980 nm) (bottom) of the wafer which was edge isolated by sawing trenches in the back side after the printing. In the LBIC map the positive effect of the emitter going around the edge of the cell is visible (bright area, top) compared to the rest of the wafer (less bright, bottom). The bad stripe in between (black) results from the trench in the back side. In addition the shunt in the corner of the wafer is visible in both measurements.

6. SUMMARY

In most solar cell processes edge isolation is an important step. In industry this is mostly done by plasma etching of a wafer stack. Because this treatment is not in-line capable and unwanted chemicals have to be used, there is a demand for alternatives. In this investigation 7 different techniques for edge isolation were examined using IV, LBIC and lock-in thermography measurements. For this experiment a batch of 100 neighbouring mc Si wafers were processed using the standard industrial type sequence used at UKN.

Plasma etching resulted in average fill factors, but due to the fact that the PECVD SiN deposition was carried out before the plasma etching, the SiN at the edges was partly etched away resulting in higher reflectance and therefore in lower I_{sc}. This is the reason why the efficiency is among the lowest.

Using a laser or a dicing saw and cutting trenches in the front side of the wafer results in the highest shunt resistance besides using sandpaper. The laser technique has the disadvantage that the saturation current density J_{02} is in the range of $6\text{-}7*10^{-8}$ A/cm² and therefore the fill factor is only 75 % and 73.6 % for lasering in the front and in the back side, respectively.

Isolation on the front side gives always an excellent shunt resistance, but sawing resulted in the highest fill factors in contrast to using a laser due to the low J_{02} value. Because the reduced active area on the front side was taken into account also the efficiency was highest.

Isolating on the back side has the advantage of a collecting emitter around the edge of the cell and therefore a 0.3 mA/cm² higher value for J_{sc}, but low fill factors have been reached due to a large amount of shunts.

There has been a good correlation between the increasing area of shunts detected with thermograms and the decreasing value of the shunt resistance. Part of the shunts could also be detected with high resolution LBIC mappings of the wafer's edge.

ACKNOWLEDEMENTS

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