SILICON LPE ON SUBSTRATES FROM METALLURGICAL SILICON FEEDSTOCK FOR LARGE SCALE PRODUCTION

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ABSTRACT

Liquid phase epitaxy (LPE) was used to deposit thin crystalline layers on multicrystalline silicon wafers fabricated from upgraded metallurgical silicon feedstock provided by Elkem. In previous investigations we reported on LPE technologies capable to grow on up to 6 layers ($12cm^2$) in a batch type apparatus. In this paper we present an up-scaling of our LPE system to a total deposition area of 0,54 m^2 per run. We report on the investigation of different barrier layers (SiO_x, TaO, TaN) deposited on one side of the wafer to avoid epi-growth on the rear. In Addition three different crucible materials (quartz, graphite and sigradur®) and different wafer carriers were tested. Explanations for an unintentionally grown oxide on the wafer surface are suggested.

1. INTRODUCTION

At the present time, most silicon wafer solar cells are fabricated from off spec material from the electronic industry and from overcapacity of EG Silicon from their component suppliers. Regarding the enormous increasing of the PV market, about 20-25% a year, a shortage of SoG-Si feedstock is expected in the years to come.

In this work an alternative way is suggested to supply the PV industry independent of the electronic chip industry. Elkem Solar is developing upgraded metallurgical silicon, which can by produced in large scale. Results in a previous EU project show [4], that upgrading the metallurgical silicon to PV-grade (PVG-Si) can be used as feedstock without the need for complex high cost chlorosilane process to purify the product. Such low cost feedstock gives a reasonable efficiency solar cell [1], provided a high purity thin silicon layer is grown on the multicrystalline substrate wafers, which is made of PVG-Si by conventional ingot casting and wafering.

In previous work we already used special arrangements of liquid phase epitaxy from indium and tin solution to grow the c-Si thin layers on this kind of substrates [1-5].

In this paper an up-scaled LPE system is introduced, capable to handle up to 54 wafers $10 \cdot 10cm^2$ per run within less than 8 hours. An industrial relevant throughput should be feasible by further enlarging the system and multiplying the LPE reactor. First batches of $10 \cdot 10cm^2$ wafers have been provided with LPE layers. Further investigations are targeted at enhancement of this technique in detail and development of the corresponding solar cell processing.

The design and operation of a batch LPE system is also discussed by K.J. Weber (ANU) at this conference [6].

2. LPE GROWTH PROCESS

The LPE process described in [1] was up-scaled as illustrated in Fig. 1. to grow on several silicon substrates and to verify whether this technique is applicable to industrial relevant wafer sizes.

We still used indium (6N) as a solvent with a small amount of gallium for higher p-type doping ($5 \cdot 10^{16}$-10^{17} cm^{-3}). The starting growth temperature was 1000°C, the cooling rate 0,5°C/min and the end temperature 900°C. However, the thermocouples have been arranged outside the process tube, therefore the temperatures in reality are lower. The wafers were loaded either single or back to back, resulting in double or single sided growth. Fig. 2 shows a one side epi-layer of 30µm thickness. At the beginning of each run the melt was saturated at 1000°C for 15min by silicon from the substrate wafers themselves and by thinning the substrates corresponding to this melt back. Additional electronic grade silicon was not needed. It is expected that metallic impurities of the substrate, if any, remain in the melt rather than to crystallize into the epi-layer. Initial the substrate wafers have been cleaned in an industrial way by NaOH etching. Etching times of about 1min (2µm) were enough as compared to 9min for the standard process because the following melt back process described above also removed the wire saw damage on the wafer surface.

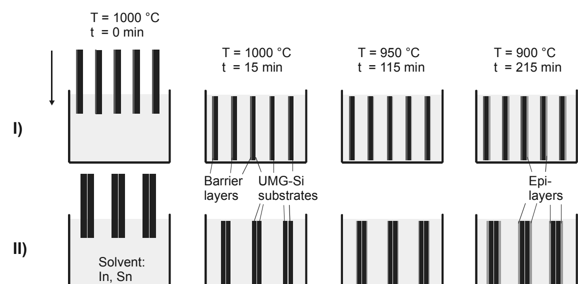

Fig. 1 silicon LPE growth principle for epi-layers on wafers from upgraded metallurgical silicon.
I) single wafers +barrier for one side deposition
II) wafers back to back for one side growth

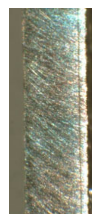

Fig. 2
As grown one side epi-layer of 30µm thickness on Elkem PVG-Si wafer

3. WAFER CARRIER DEVELOPMENT

The most important task in this work was the development of a wafer carrier for the new geometry of the LPE-System. In a first trial a home made carrier for 19 wafers 5·5cm^2 was built from quartz glass rods, shown in Fig. 2.

Fig. 2 Carrier for 19 wafers 5·5cm^2 in load lock

With this carrier we investigated the quality and usability of a set of different growth barrier layers, deposited onto one wafer surface to prevent LPE growth on the back side of the solar cell. Details are described in the next chapter. Soon it was obvious, that a more capable sample carrier was needed, which e.g. has to be removable from the load lock to simplify the wafer handling.

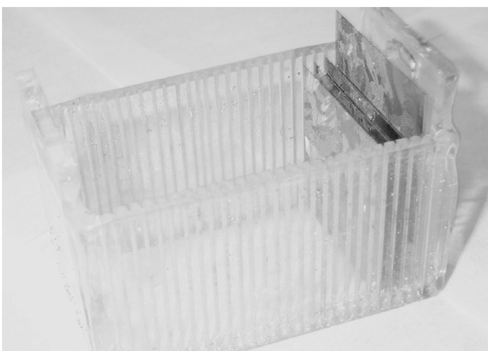

Fig. 3 Removable carrier for 25 wafers of 5·5cm^2

The quartz carrier shown in Fig. 3 enabled to load the wafers outside the apparatus and gave the possibility to be placed into the load lock in an easy way. While first deposition experiments were carried out, a carrier for wafers of 10·10cm^2 has been developed. The requirements for this carrier were as follows:

- The carrier has to be removable from the load lock to simplify the wafer loading.
- Wafers of at least 10·10cm^2, as much as possible, have to match into the carrier.
- The carrier must fit into the given cylindrical crucible limited by the dimensions of the furnace and the process tube.
- It must ensure the possibility of back to back loading the wafers to avoid growth on the rear.
- The right proportion between wafer deposition surface and volume of the melt should be fulfilled. Distances of 2-4mm between the wafers are suitable for single sided growth.
- The material must resist temperatures of up to T=1050° and must not lead to contamination of the melt.
- The solvent should drop off during unloading the carrier from the crucible.
- Slow rotation of the carrier must be possible for better temperature homogeneity and disturbance of the melt during growth.
- The system must enable cooling rates of 0,1 -0,5°C/min

From this considerations a virtual model was designed (Fig. 4). Afterwards the first model has been constructed from plastic material and now a graphite carrier is finished, with improvements in detail, which fulfilled the requirements mentioned above. It enables to process LPE-layers of up to 0,54m^2 in one run, if 2mm distance between the wafers is chosen and 0,28m^2 for 4mm distance respectively. With the 4mm distance we achieved first success leading to homogenous LPE layers on low cost multicrystalline upgraded metallurgical silicon wafers. Further developments of this carrier are underway, e.g. a more exact positioning of the carrier within the crucible to achieve higher reproducibility.

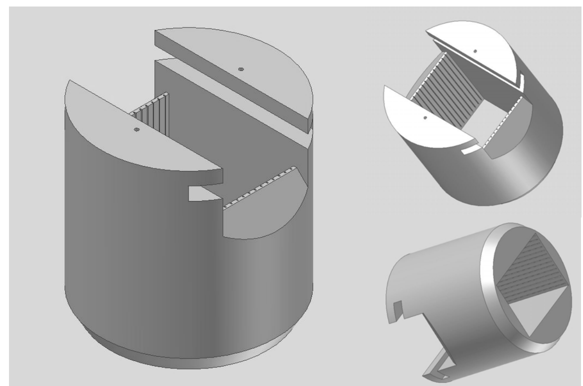

Fig. 4 Model of carrier for up to 54 wafers 10·10cm^2. This picture shows only 14 slots. The real carrier has 27 slots for 54 samples, each two wafers back to back.

While carrier development three different materials have been used for the carrier and the crucible respectively: Quartz glass, graphite and sigradur® (only for crucible). Initial there have been problems with unintentionally deposited SiO_x and indium oxide at the melt surface and on the silicon wafer before dipping. The oxidation could be avoided after both crucible and carrier have been made from graphite of semiconductor quality and the graphite

was annealed in inert gas for several hours and no more exposed to the air for more than a few minutes.

Thus it was confirmed, that the oxidation problems were due to the crucible and carrier materials and not due to the protective gas (Ar, H_2) or the apparatus itself. The indium solvent seems to act catalytic for reactions between solved silicon and quartz glass or sigradur® respectively to harmful oxide on the wafer surface before LPE growth.

4. BARRIER LAYERS

To prevent epi-growth on the rear side of the wafer, a set of different growth barrier layers have been deposited by German partner institutes and LPE was investigated on the front side of these samples. All the barriers fulfill the following requirements:

- Close layer of about 100nm thickness (for back to back lower thickness or even no barrier is needed)
- Stability at temperatures up to 1000 °C
- Resistance against liquid solvent (In) at 1000 °C
- Resistance against HF-dip (2%, 2min) for natural oxide removal on the front side

The barrier layers investigated in this work are listed in Table I. The SiO_x layers deposited by PECVD at the Institute for Plasma Research at the University of Stuttgart showed excellent characteristics. No silicon deposition was observed after growth and the indium solvent completely dropped down during unloading the wafers. Similar results were obtained from the SiO_2 barriers deposited by sol-gel coating at the institute for new materials of the Saarland University. Initial adhesion problems of SiO_2 on the wafer surface during dipping into the sol-gel have been solved. However, spin coating would be more favourable as compared to dipping.

The Semiconductor and Microsystems Technology Laboratory at the Dresden University of Technology (IHM) provided TaN, TaSiN, TaO, TaSiO barrier layers by sputtering. We found that TaN, TaSiN and TaSiO layers were useful candidates to prevent epitaxial growth on the rear. However, the surface was not completely free from deposited silicon and indium solvent respectively (see Fig. 4, right picture, upper left corner). For back to back mode these barriers may be applicable. In contrary TaO resulted in excellent clean and non coated rear surfaces (Fig. 3 left side).

The usability of the growth barrier seems to correlate with the resistivity of the materials investigated (see Table I.). The conductivity of the Ta(Si)O and Ta(Si)N barriers would allow simple rear side contact formation eg by bonding an aluminium foil onto the wafer surface.

Table I. Rear side barrier layers deposited by different methods at our German partner institutes.

Growth barrier	Partner Institute	Deposition method	Resistance [Ωcm]
SiO_x	IPF Stuttgart	PECVD	-
SiO_2	INM Saarland	Sol gel	-
TaN	IHM Dresden	Sputtering	$2 \cdot 10^{-3}$
TaSiN	"	"	$2 \cdot 10^{-4}$
TaO	"	"	1
TaSiO	"	"	0,1

In addition all barrier layers act as effective phosphorous diffusion barriers which might be of advantage during further solar cell processing.

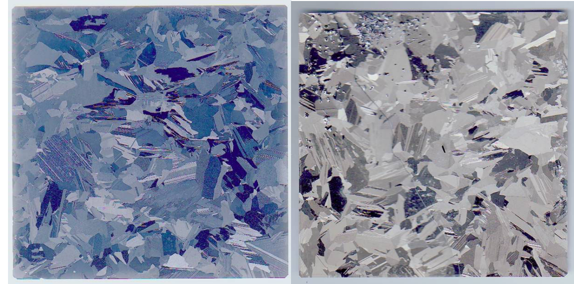

Fig 4: Rear surfaces of 100cm^2 wafers after LPE process with barrier layers. Left: clean SiO_x surface; right: TaSiN, damaged at upper left corner

5. APPLICATIONS OF LPE LAYERS

In previous investigations [5] we demonstrated, that both p-type and n-type layers in a wide range of dopant concentrations can be grown by LPE from In, Sn and Ga solutions. Especially n-type epitaxial silicon is achieved even when cheap Sn (3N) is used as a solvent, as the major impurities are Sn, As, Bi in this case. Hence the currently running and further planed activities with the newly developed high throughput reactor are the following:

5.1 P-Type Absorber Layers

Epi-layers from indium plus a small amount of gallium solvent grown on highly boron doped multikrystalline PVG-Si (upgraded metallurgical silicon) substrates. The melt back provides the purification of silicon dissolved in the indium melt as well as cleaning the substrate surface.

5.2 P^+-Type BSF Layers

The back surface field (BSF) can also be realized by LPE. Thin highly doped p^+-type layers may be grown from In/Sn/Ga solvent for e.g. thin (<200µm) mc silicon wafer solar cells with the advantage of low process temperature and high throughput because of small distance between wafer pairs during deposition process. In this way gallium could substitute boron to prevent high temperature and carrier induced degradation respectively.

5.3 N-Type Absorber Layers

N-type epi-layers can be grown from cheap Sn solvent, as the residual impurities As, Sb and Bi act as n-type dopants. As there are much more highly doped CZ wafers available from n-type silicon scrap from electronic industry as compared to p-type wafers, the layers should be grown on such highly doped n-type wafers as a substrate.

5.4 P^+-Type emitters

Similar to the BSF described above, LPE also can be used for deposition of highly doped p-type emitter layers from In/Sn/Ga solvent for n-type solar cells. The advantage would be the low process temperature of 800-850°C as compared to temperatures above 900°C needed for boron emitter diffusion, which might crack the mc material.

6. CONCLUSION

It was demonstrated that LPE can be carried out on several wafers 10·10cm^2 in a vertical batch system. It has still to be investigated whether the substrate wafers should be loaded single or back to back. Besides standard PECVD-SiN a set of possible growth barrier are presented. However, for back to back growth it has still to be investigated, whether the barrier layers are needed.

Planed applications are LPE absorber layers on mc-Si wafers made from low cost PVG-Si feedstock. Other possible applications, enabled by the up scaled LPE System, are mentioned in this paper.

7. ACKNOWLEDGEMENTS

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