PLASMA TEXTURING AND ITS INFLUENCE ON SURFACE PASSIVATION

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ABSTRACT: In this paper a proof of concept of a plasma texture developed for solar cell processing is presented. Currently the implementation of this step into standard cell processes is limited by the uniformity of the etching results. It was, however, successfully introduced into a photolithography based process for 2x2 cm²-cells, leading to a benefit in efficiency of up to $1\%_{abs}$ compared to untextured samples. The combination with emitter passivation by thermal oxide on the front side – both steps apart from each other leading to an improvement of cell data – shows a degradation of the effective diffusion length. This detrimental effect is assigned to defects generated at high oxidation or firing temperatures and demands further investigation and adjustment of the processing steps.
Keywords: Texturisation, Plasma Etching, Passivation

1 INTRODUCTION

Opposite to wet texturing methods, plasma processes feature less dangerous handling, easier waste disposal, reduced use of deionized water [1] and single-sided etching permitting new rear side concepts [2]. Moreover, they offer new possibilities for multicrystalline materials without saw damage, like EFG, which can not be processed using common chemical texture methods.

2 PLASMA TEXTURING

In this work a plasma texturing process for silicon wafers was developed using a remote chemical downstream etcher (ASYNTIS Pioneer 1). In the Pioneer, the plasma is ignited by a microwave source situated above the reaction chamber, which allows the ions to be trapped before reaching the sample. In contrast to Reactive Ion Etching (RIE), there is no acceleration of ions by a bias voltage. Reactions on the silicon surface are carried out by radicals. This reduces plasma-induced damage and leads to isotropically etched surfaces. Currently a gas mixture of SF_6 and O_2 is used. The silicon is removed from the surface mainly via the following reaction

$$4F\cdot + Si \rightarrow SiF_4$$

Adding oxygen is understood to accelerate the etching process by providing more fluorine radicals via

$$SF_6 + O\cdot \rightarrow SOF_4 + 2F\cdot$$

Once the amount of oxygen is further increased, however, the etch rate is slowed down due to the formation of a $Si_xO_yF_z$-film. The good selectivity of fluorine, removing silicon but not silicon oxide, causes the randomly distributed film to act like a mask. This self-masking leads to a sponge-like surface morphology.

The Pioneer was originally used for providing edge isolation in the standard screen-printing based solar cell process at University of Konstanz (UKN). Starting with the process for edge isolation the plasma texture recipe was obtained mainly by decreasing the gas flow, moreover by adjusting the SF_6/O_2 ratio and also by implementing preceding cleaning steps. It was optimized for low reflectivities on EFG material and applied to various wafer types. Scanning Electron Microscope (SEM) images (figure 1) show feature sizes around 200 nm, which lead to a reflectivity around 20% (weighed spectral reflectance between 300 and 1200 nm without anti-reflective coating (ARC)), regardless of the wafer type (EFG, mc, FZ, Cz).

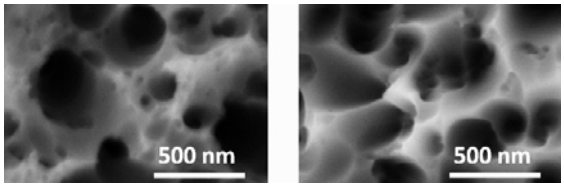

Figure 1: SEM images of the surface structure obtained by plasma texturing on common multicrystalline (left) and EFG (right) wafers

Since the feature size is smaller than the wavelength of visible light, diffraction effects have to be considered [3]. Two-dimensional simulations hint, that feature sizes around 400 nm are best suited to reduce reflectance without causing severe surface recombination losses [4]. Larger feature sizes can be obtained by adding chlorine, which etches anisotropically depending on the crystal orientation [2].

Spatially resolved reflectivity measurements reveal sufficient uniformity for areas smaller than 12.5x12.5 cm², see figure 2. Better homogeneity is difficult to obtain due to the geometry of the reaction chamber, currently limiting the implementation of plasma texturing (PT) into standard cell processing using the Pioneer.

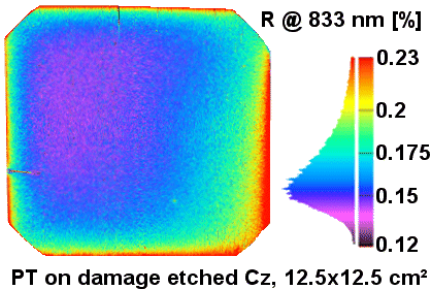

Figure 2: Spatially resolved reflectivity measurement to analyze the uniformity of the texture process

3 CELL PROCESS IMPLEMENTATION

The developed plasma texturing step was introduced into a photolithography-based solar cell process as outlined in figure 3.

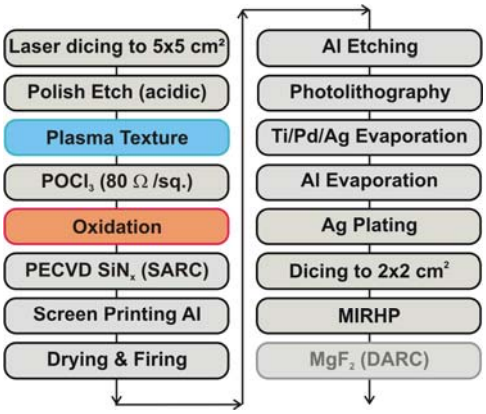

Figure 3: Cell process used in this study

During the texture process only around 2-3 µm of Si are removed from the surface. It turned out that an acidic polish etch before plasma texturing is essential to obtain a uniform plasma etch result. Optionally a thin thermal oxide was grown onto and into the wafers with the goal to obtain better surface passivation. Thereby neither the morphology nor the reflectivity changes significantly. The deposition of 60-70 nm PECVD silicon nitride as Single layer Anti-Reflective Coating (SARC) smoothly follows the surface structure whereas additional MgF_2-evaporation leads to small cracks (figure 4).

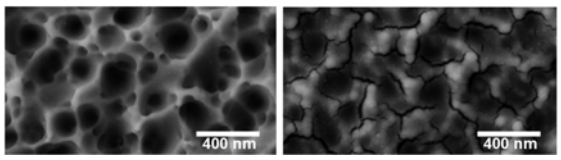

Figure 4: SEM images of plasma-textured surfaces with single anti-reflective layer (left) and double anti-reflective layer (right)

Generally speaking the value of the weighed reflectivity is halved by the plasma texture compared to flat wafers, with or without anti-reflection coatings (figure 5).

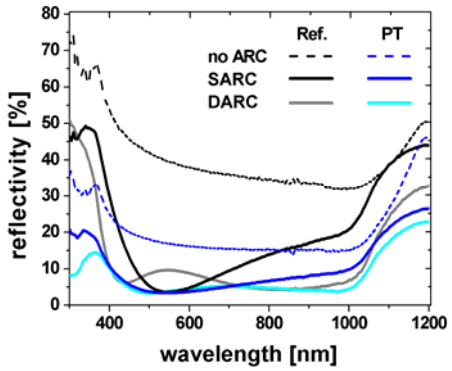

Figure 5: Comparison between the reflectivities of plasma-textured wafers and non-textured references on FZ material, also with single anti-reflection coating (SARC) and double anti-reflection coating (DARC), respectively

Without a second anti-reflection coating, an improvement in cell efficiency of up to $1\%_{abs}$ is possible, see table I.

Table I: Cell data showing a benefit by plasma texturing of up to 1% in efficiency compared to untextured cells from the same wafer (0.8 Ωcm FZ, cell thickness 240 µm). This data was obtained using the above outlined photolithography-based cell process with SARC only.

wafer type	plasma texture	FF [%]	j_{SC} [mA/cm²]	V_{OC} [mV]	η [%]
FZ	No	79.1	33.5	638	16.9
FZ	Yes	80.0	35.2	637	17.9

4 INTERACTION BEWEEN PLASMA TEXTURE AND SURFACE PASSIVATION BY THERMAL OXIDATION

Emitter passivation by a thin thermal oxide underneath the PECVD SiN_x showed improvement of cell data on untextured cells [5]. The same effect was expected for plasma-textured wafers. Instead, the combination of these two steps resulted in decreased cell efficiencies, as listed in table II.

Table II: Results of neighbouring cells on different plasma-textured materials with and without thermal oxide. This data was obtained according to the above outlined photolithography-based cell process with SARC only.

wafer type	Oxide	FF [%]	j_{sc} [mA/cm²]	V_{OC} [mV]	η [%]
EFG	No	78.6	33.3	591	15.5
EFG	Yes	77.3	30.1	559	13.0
mc	No	80.2	34.4	626	17.3
mc	Yes	80.0	34.6	622	17.2
FZ	No	80.5	35.0	630	17.8
FZ	Yes	80.2	33.1	613	16.3

Compared to flat wafers spectral response data shows degradation in the blue response area on plasma-textured wafers due to surface recombination, as already shown in [6]. As expected, thermal oxidation leads to increased values of Internal Quantum Efficiency (IQE) at short wavelengths due to better emitter passivation. On the other hand, oxide on plasma-textured samples results in a lower IQE at long wavelengths. The reduced effective diffusion length is understood to be caused by defects generated at high oxidation or firing temperatures in combination with plasma texturing. This detrimental effect is less pronounced on the high quality mc material used compared to common EFG.

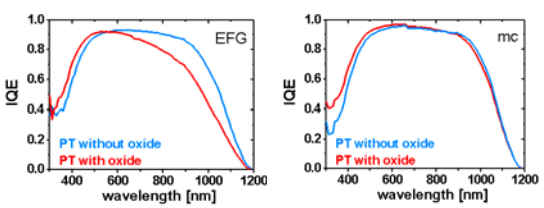

Figure 6: Spectral response of plasma-textured neighbouring EFG/mc cells (cell data listed in table II)

An explanation for the degradation of the plasma-textured cells with thermally grown oxide could be the dissociation of precipitates during oxidation. On the other hand the degradation is also visible for very clean plasma-textured FZ samples as well as for cells without plasma texture, so precipitations should not play the major role at least for the FZ cells. Another reason might be thermally induced stress [7], although the feature size of the texture is very small.

For a better understanding measurements of the Quasi-Steady State Photo Conductance decay (QSSPC) on Czochralski material were carried out. For this the samples were symmetrically processed with texture, oxide and nitride on both sides. Before the SiN_x firing step for hydrogenation, oxidized wafers showed lower values of emitter saturation current j_{0e} than non-oxidized samples. Whereas non-textured, oxidized wafers further improved after firing, plasma textured ones deteriorated, exceeding the values of non-oxidized wafers. After hydrogenation in microwave induced remote hydrogen plasma (MIRHP), the emitter saturation current decreased, but still did not reach the level before firing. No significant effect could be observed after applying another MIRHP step, which could be a hint for sufficiently optimized hydrogenation. A second firing step followed by a MIRHP step, however, led to an improvement of the oxidized wafers. Typical results are shown in figure 7.

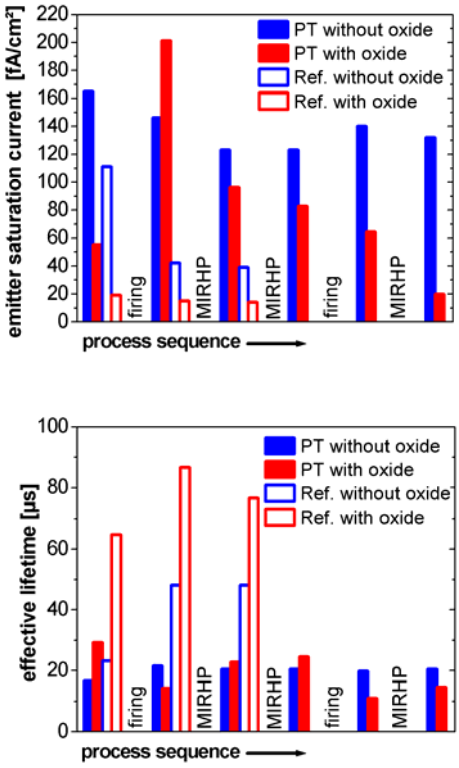

Figure 7: Emitter saturation current density of plasma textured wafers with and without thermal oxide after different firing and MIRHP hydrogenation steps (top) and mean effective lifetime accordingly (bottom)

While raising new questions concerning the firing process this data is consistent with the improvement in blue response shown above.

The effective lifetime data was taken from the QSSPC measurements as well. Compared to flat references the effective lifetime shows a significant decrease on plasma-textured samples. First carrier lifetime measurements show no degradation in bulk lifetime by thermal oxidation of textured samples. This could be a hint that defects occur during the firing step or that the effective lifetime deteriorates because of surface effects.

5 SUMMARY AND OUTLOOK

A plasma texturing process was developed and implemented into a photolithography-based solar cell process, leading to low reflectivities and good cell efficiencies on various wafer types. The interaction of plasma-textured surfaces with a thin thermal oxide results in lower cell efficiencies – a phenomenon which is not yet fully understood showing the importance of adjusting the surface passivation for plasma-textured wafers.

Further experiments include QSSPC measurements of different plasma textures and wafer types to obtain better statistics. IV-curves may help to distinguish between the contributions of bulk, emitter and depletion region. Bulk effects will be further investigated using lifetime measurements on plasma-textured samples with a thin thermal oxide after different treatments.

6 REFERENCES

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