IMPACT OF THE CRYSTAL STRUCTURE ON SOLAR CELL PARAMETERS OF RIBBON GROWTH ON SUBSTRATE (RGS) SOLAR CELLS

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ABSTRACT: Ribbon Growth on Substrate (RGS) is a cost-effective method to produce silicon wafers directly from molten silicon without material losses due to wire sawing. This technique decouples crystallization and pulling direction of the silicon wafers which results in good wafer quality at a very high production speed of about one wafer per second. The multicrystalline wafers have typical grain sizes between 0.1 mm and 0.5 mm so that spatially resolved investigations of the effect of the crystal structure on cell performance are expected to improve wafer production and cell processing. One processed RGS solar cell was measured with Light Beam Induced Current (LBIC) and Lock-In Thermography (LIT) and the data was correlated with dislocation densities and electron microscopy investigations. In regions where the as grown wafer is thinner compared to the average wafer thickness, the internal quantum efficiency shows a tendency towards lower values. This can be traced back to high defect densities introduced by mechanical stresses during casting. An Energy Dispersive X-ray (EDX) analysis revealed carbon and oxygen impurities and possible precipitates. Also metal impurities in some of the defect-rich regions were found which may affect their electronic properties.

Keywords: Ribbons, Dislocation, Characterization

1 INTRODUCTION

Ribbon Growth on Substrate (RGS) [1] is a cost-effective approach to face main issues in the photovoltaic market such as feedstock shortage, increasing wafer demand and development of high throughput production technologies. This method is based on growing silicon wafers directly on a substrate. Unlike the common ingot technology there are no losses due to wafer sawing. As shown in figure 1 the crystallization and pulling direction are decoupled which results in a very high production speed in the order of one wafer of a size of 156x156 mm^2 per second [2]. Preheated substrate plates are transported underneath the molten silicon inside a casting frame. The wafers crystallize on reusable substrates which absorb the crystallization heat. The wafer thickness is adjustable in a wide range via process parameters such as the wafer pulling speed.

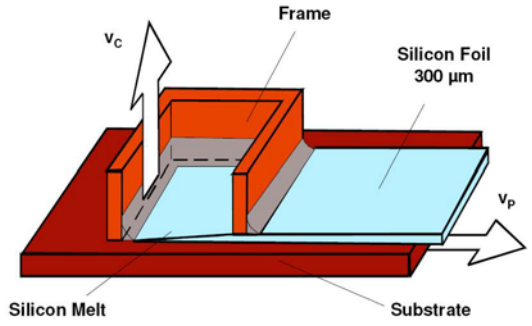

Figure 1: Illustration of the RGS production principle, indicating pulling direction v_p and crystallization direction v_c [1,2].

RGS wafers are produced up to now by a laboratory scale, batch type machine at ECN Solar Energy for research purposes only. Currently RGS Development B.V. is developing a first continuously operating prototype machine, which is in the start-up testing phase at the moment. (see Figure 2).

Figure 2: RGS production machine installation at RGS Development B.V.

A consequence of the fast crystallization is that the wafers suffer from higher crystal defect densities such as dislocations, grain boundaries and impurities which limit the as grown minority charge carrier lifetimes [2,3]. To improve the as grown wafer quality, fundamental knowledge about the crystallographic and electronic properties of RGS wafers and their impact on solar cell performance is necessary.
In this work spatially resolved measured parameters of a RGS test solar cell, e.g. the internal quantum efficiency and the spatial distribution of heat dissipating areas were correlated with corresponding crystal thickness and structure.

2 CELL PROCESS AND CHARACTERISTICS

In this work a specific RGS test solar cell was chosen that showed a wide variety of areas with different material qualities. This enables to directly compare regions of lower and higher density of material quality limiting defects which reduce the internal quantum efficiency (IQE) and the carrier lifetime.
The wafer under investigation is boron doped (3 Ωcm) and has relatively low interstitial oxygen [O_i] concentration in the range of 3-5*10^{17} cm^3. The cell

process chart is shown in figure 3. For an optimized processing this wafer was mechanically planarized with a special tool prior to emitter diffusion. This step leads to a wafer thickness due to the the planarization height.

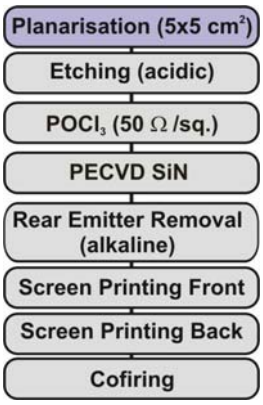

Figure 3: Process chart of the investigated cell.

Depending on the planarization depth, there are still regions on the wafer that are thinner which remain unplanarized. For the selected cell, these regions appear as a lengthy pattern in the pulling direction of the wafer during crystallization and can be seen in the Light Beam Induced Current (LBIC) measurement in figure 4. The material quality tends to be lower in these thinner regions (area 1 in figure 4) showing a lower IQE. After planarization the industrial type screen printing process was applied, which includes acidic etching, phosphorous diffusion and SiN_x coating. To avoid RGS specific process induced shunting [4] a screen printed Al-grid with only 10% coverage was applied on the backside. This is why the parasitic backside emitter was removed by alkaline etching prior to metallization. As shown in table 1 this cell process results in a solar cell efficiency of 11.5%.

Table I: IV parameters of the RGS solar cell under investigation.

Efficiency	Voc	Jsc	FF
11.55 %	582 mV	28.5 mA	69.5%

3 ELECTRONIC CHARACTERISATION

The cell under investigation was mapped with LBIC and examined with illuminated (iLIT) [5] and dark Lock-In Thermography (dLIT) [6]. The obtained images show a correlation between the local IQE and the corresponding wafer thickness. It is found that thinner regions of the wafer show a tendency towards a lower IQE as shown in figure 4 in area 1. More interesting, however, are the neighboring wafer areas that unexpectedly show a significantly better IQE while sharing the same lengthy pattern parallel to the pulling direction like area 2 in figure 4.

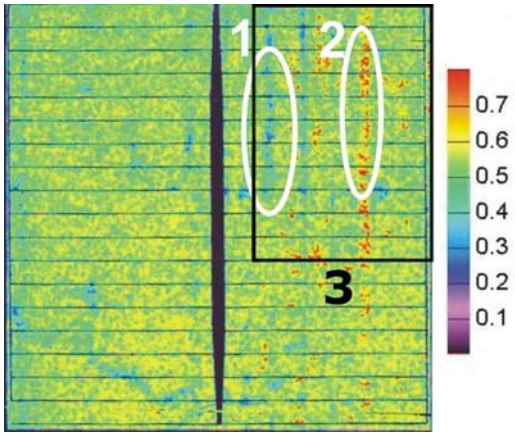

Figure 4: LBIC map of the cell with areas of lower (1) and higher (2) IQE at 980 nm.

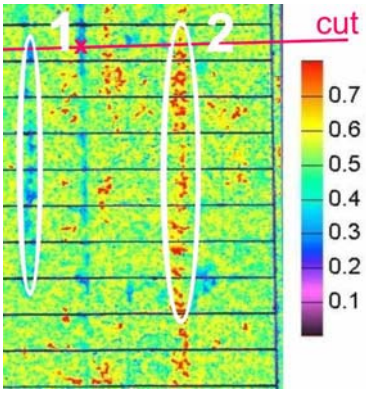

Figure 5: High-Resolution LBIC scan of frame 3 in figure 4. This section was investigated with the LIT technique as well. The red line indicates the cutting direction of the edge samples shown later.

To obtain additional information, the LBIC image was compared to an iLIT image which is an excellent tool for shunt detection. Besides stronger point shunts there are several thermal signals in the vicinity of area 2 in figure 6 that show heat dissipation.
By comparing the obtained iLIT and dLIT images different shunt types can be distinguished, such as ones with ohmic or Schottky-type behavior. With dLIT carried out under forward and reverse bias, horizontal ohmic shunts between the back side grid fingers can be ruled out as process induced [4] while the vertical pattern of Schottky-type shunts seems to be related to the vertical pattern found in the LBIC measurements as depicted in figure 4, region 2.

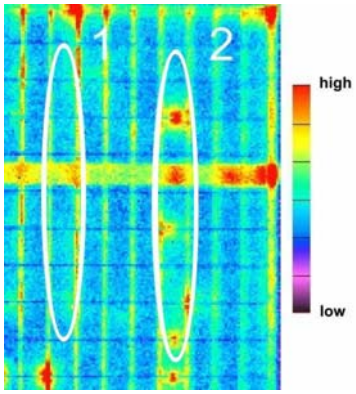

Figure 6: Frame 3 of figure 4 investigated with iLIT under V_{oc} condition. The brighter lines are the backside grid fingers.

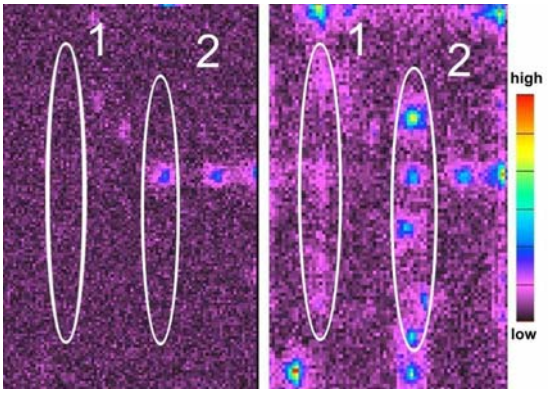

Figure 7: Frame 3 of figure 4 investigated with dLIT under reverse (left) and forward (right) bias.

By comparing area 1 and 2 (i.e. thinner and thicker crystal areas) of figure 4 (IQE) with the corresponding areas in figure 6 and 7 (dLIT), it is found that both crystal fractions (area 1 and 2) seem to dissipate heat due to enhanced recombination as a result of crystal defects. However, the dLIT signal is weak and has to be further investigated. On a first glance, it seems that the thicker crystal fraction (area 2) produces a higher dLIT signal which shows in addition a Schottky-type behavior.

4 CRYSTALLOGRAPHIC PROPERTIES

After characterization the metallization, ARC and emitter were removed by wet chemical etching and then the wafer was diced into samples. The edges of the samples were polished for crystallographic investigations. In the following pictures we present horizontal cuts perpendicular to the regions 1 and 2 in figure 4. Grain boundaries and defects were visualized by Secco etching [7]. The so gained visible crystal structure was compared to the corresponding IQE signal obtained by LBIC as shown in figure 8.

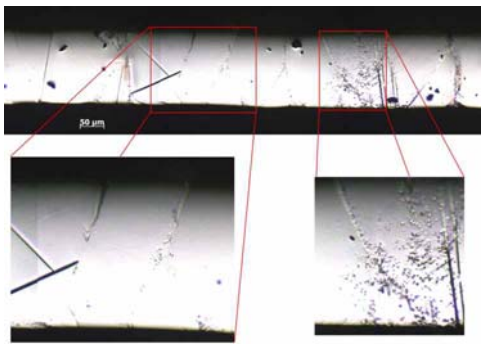

Figure 8: Wafer cut between region 1 and region 2 at the transition between an electronically good region (left) and a region with lowered IQE (right). The large black spots on the surface in the upper image are artifacts from the sample preparation.

The picture indicates a correlation between electronic properties and the defect density. This correlation becomes even more instructive if we compare the IQE linescan readings with the average defect density along the wafer as can be seen in upper picture in figure 9. Areas with higher defect density result in a lowered IQE. However, the bottom picture shows a deviation which is explained later.

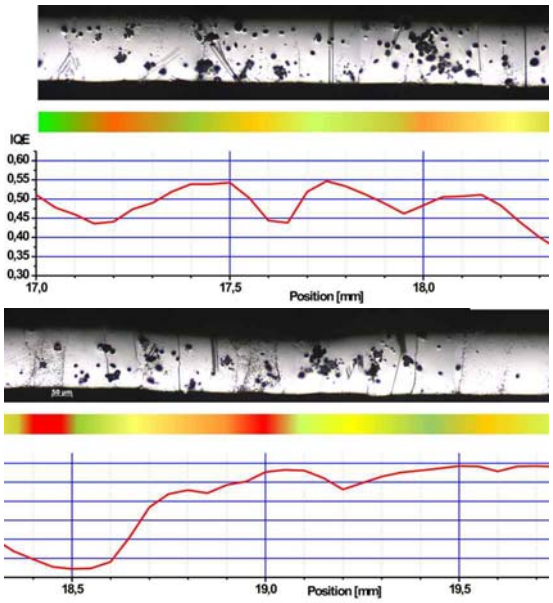

Figure 9: Wafer cross-section over the quantum efficiency linescan across region 1 along the cut as shown in figure 5. The color bar represents the visible defect density and is just a guide to the eye from green to red (a.u.).

The crystal structure in terms of the RGS specific columnar grain boundaries seems to have only a small influence on the quantum efficiency.
Further investigations therefore concentrate on regions with high defect density in the wafer areas where differences in height and IQE occur. These elongated regions originate from the pulling process and continue over centimeters along the wafer as one can assume with region 1 in figure 4. This region is examined closely in figure 10.

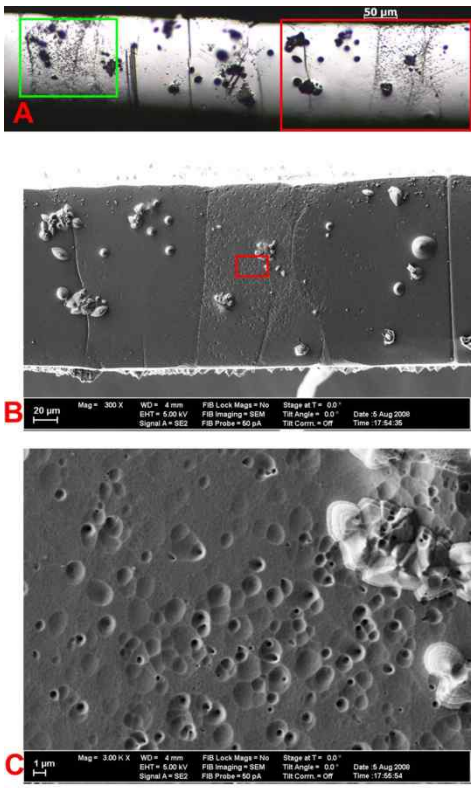

Figure 10: A: microscopic picture of a cross-section of region 1. B: red region of A magnified under the electron microscope. C: further magnified view to visualize the etch pit density, which in this area is up to $5*10^7$ etch pits per cm²

However, sheer defect density does not seem to explain the whole electronic behavior. On the left side of figure 9 there is an area with comparable defect density (figure 10A outlined in green) but with significantly less detrimental impact on IQE (Position 19 mm in figure 9).
For the defects an additional factor like precipitates or metallic impurities has to be assumed to influence the electronic properties, especially when looking at the area with the lowest IQE of this sample as depicted in figure 11:

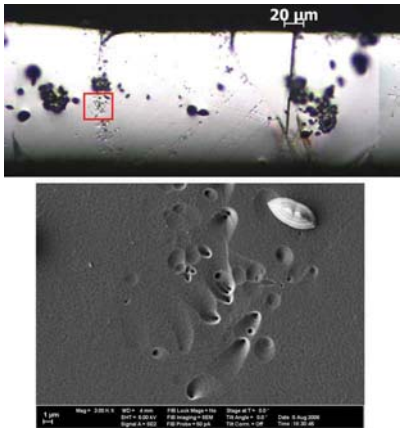

Figure 11: The upper picture shows the cross section area between region 1 and 2 with the lowest IQE, marked with an x in figure 5. The bottom picture is a SEM image of the etch pits within the red box with a density around 10^7 etch pits per cm²

The defect density is significantly lower than expected from the LBIC IQE readings, so an Energy Dispersive X-ray analysis (EDX) was carried out to determine the elemental composition of the sample at this point.
A relatively high carbon content was found which is not uncommon for this material due to graphite parts used in the casting environment. Noticeable, however, were the traces of tin we also detected in this surrounding. This could be a unique contamination since tin was never before detected in RGS material. The inhomogeneous distribution serves as a hint that defects may attract carbon and metallic impurities (internal gettering) which furthermore degrade the quantum efficiency [8].

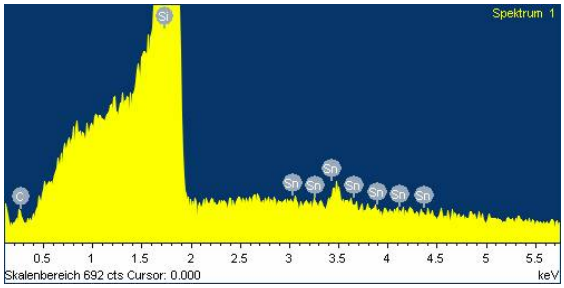

Figure 12: EDX spectrum of the area depicted in figure 11. Several L-lines of tin on the right side of the picture could be identified and an estimation results in a local concentration of 0.3 – 0.4 mass-% next to an elevated carbon content of up to 2 mass-%

Since carbon may form rectifying needle-like structures in Si [9], it is assumed that the Schottky-type dLIT signal in region 2 (figure 7), which is not related to Al spiking because it does not occur under an Al-grid finger, originates from the detected carbon. However, it is still unclear why such a shunting behavior occurs preferably in regions with good IQE and moderate defect density. One explanation could be that the carbon forms current collecting channels which result in a higher IQE as suggested in [9] and [10]. This is supported by another EDX analysis which detected a higher oxygen content in region 2 relative to the other areas of the wafer.

5 SUMMARY

RGS has advantages in wafer production compared to standard block cast material, due to the avoidance of wafer sawing losses and a very fast production speed. As a result of the fast crystal growth, the material may suffer from various crystal defects. A RGS solar cell, processed according to an industrial type screen printing process, was investigated using spatially resolved measurement techniques like LBIC and Lock-In Thermography.
After cutting the wafer across the regions of interest, the grain structure, the dislocation and the defect density was investigated in detail. Regions with the most deviating LBIC signal were analyzed using an electron microscope and Energy Dispersive X-ray analysis (EDX). In many cases correlations between the local defect density of the material and its corresponding electronic properties were found while the grain structure seemed to be of less importance to the IQE. Additionally, it was found that

the crystals with the lowest IQE contain traces of metallic impurities around their defects.
One can conclude that in regions where the as grown wafer is thinner compared to the average wafer thickness, dislocations, defects and impurities amass and the internal quantum efficiency shows a tendency to lower values.
The results of this paper demonstrate the importance of defect characterization and analysis in the development of new silicon materials such as RGS. This knowledge is very helpful as a feedback to further improve wafer production and solar cell processing. In the test sample analyzed in this paper, it implies that process inhomogeneities during casting result in an inhomogeneous wafer height and in locally introduced stress. This has to be minimized since defects and dislocations introduced by the stress do not only serve as a sink for minority charge carrier but may also accrete impurities.

6 ACKNOWLEDGEMENTS

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