N-TYPE MULTICRYSTALLINE SILICON: MATERIAL FOR SOLAR CELL PROCESSES WITH HIGH EFFICIENCY POTENTIAL

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ABSTRACT

We present the characterisation of directionally solidified n-type Si ingots. Three ingots with a range of bulk resistivities and different n-type doping elements (Sb, P and As) were studied. We show from Hall measurements that the mc-Si material has excellent electrical transport properties. The mobilities are close to the theoretical limit, which is given mainly by scattering at acoustical phonons. Mobilities so close to the theoretical value have, to our knowledge, not been demonstrated for comparable p-type mc-Si wafers. Additional measurements on high quality p-type mc-Si material support this statement. This means that other scattering mechanisms reduce the mobility in p-type mc-Si material, but are not present in n-type silicon.

Lifetime measurements were conducted by µW-PCD using an iodine-ethanol surface passivation. This passivation was used preferably to SiN_x, as in some experiments the hydrogen from the PECVD SiN seemed to passivate the bulk at deposition temperatures. Average values in excess of 120 µs over large areas were measured.

In order to exploit the good material properties of n-type mc-Si, solar cell concepts must be developed and the processes optimised. B-diffusion is the most problematic step as it is considered to be both destructive to material quality and energy consuming. In this paper, we show that a BBr_3-emitter diffusion is possible at moderate temperatures without degrading the carrier lifetime of the mc-Si material. An additional contribution from Libal et al. [1] on solar cell processing is included in this conference.

INTRODUCTION

The rapid growth of the silicon PhotoVoltaic (PV) industry (annual rate about 30%) faces a bottleneck in the near future: the supply of Si-feedstock for wafer production. Even today the PV sector has been using purified Si intended for the microelectronics industry in addition to the p-type off-spec material [2], benefiting from the bad situation in this sector. As a recovery of demand from the electronics industry is taking place, new sources of Si must be assured in order to guarantee an unhindered growth of the PV sector.

There is the possibility to double the annual off-spec Si available for PV by using the n-type off-spec Si which is not yet utilised. The n-type off-spec material is approximately 2000 tons per year and could help to reduce the feedstock bottleneck.

For this purpose, industrial n-type Si solar cell concepts must be developed and optimised on this new material. The reason why the Si PV industry is mainly dominated by p-type solar cells can be understood by looking at the early time of PV applications. At that time, PV was used almost exclusively for space applications and as p-type Si is more resistant to radiation levels in space, p-type solar cell concepts on FZ-Si material were developed. When the solar cells were cheap enough to be attractive for terrestrial uses, the p-type route was followed as the infrastructure was already in place and the processes optimised.

At present there is a strong suspicion, confirmed by a increasing number of authors [3, 4] that n-type Si tends to be superior to p-type Si at a certain impurity (O, Fe, …) level. For example, the lack of B-O complexes makes n-type material more resistant to light- or carrier induced degradation. In addition, it was found that n-type Si is less sensitive to many impurities typically found in crystalline Si [3].

The European project NESSI deals with the purification of n-type off-spec Si-material and with the optimisation of solar cell concepts designed for n-type mc-Si. In this paper, we show that material blended from virgin and off-spec n-type doped silicon that was made for reference purposes is of very good quality, which, to our knowledge, has not yet been reported for comparable p-type mc-Si.

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EXPERIMENTAL TECHNIQUES

Directional solidification and wafer characteristics

The mc-Si material was directionally solidified at Deutsche Solar. The solidification was carried out in a HEM furnace using virgin Si-material from the electronic industry and blended with highly doped n-type Si-pieces. Three ingots with different resistivity ranges and different doping elements were grown. Table 1 summarises the properties of the wafers from these ingots.

ingot	dopant	wafer size [cm^2]	thickness [μm]	# of wafers in column
A	Sb	12.5 x 12.5	275	306
B	P	12.5 x 12.5	340	396
C	As	12.5 x 12.5	275	274

Table 1: Wafer characteristics of the three grown ingots.

Resistivity measurements were performed using the 4-point probe through the entire columns taking the average from 5 different positions on each wafer. Figure 1 depicts the distribution of the specific resistivity as a function of the position within each column. For ingot A and B the specific resistivity is in a range that is interesting for PV applications (between 1.3 Ohm-cm to 0.3 Ohm-cm) whereas ingot C was grown for comparison reasons only.

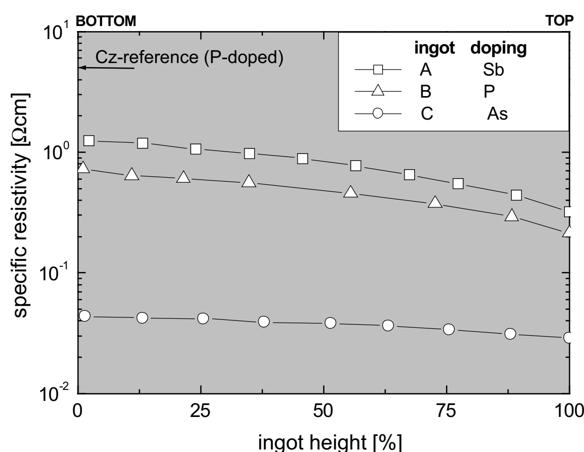

Figure 1: Distribution of specific resistivity in columns from ingots A, B and C.

Three different positions in the columns were characterised by Hall measurements. In addition, lifetime measurements on 12.5x12.5 cm^2 wafers were carried out and solar cells have been processed from ingot B. The results are described in an additional paper at this conference [1].

Measurements of electrical transport properties

Hall measurements

Hall measurements were performed to examine the electrical transport properties of the n-type wafers. The parameters were measured between 40 and 400 K on samples in van der Pauw geometry. The sample temperature was measured by a thermocouple mounted in the sample chamber a few millimetres from the sample. Thermal equilibrium was achieved by flowing expanded helium gas through the sample chamber. Ohmic contacts were achieved by the application of an aluminium paste in the case of p-type Si and an Ag paste in the case of n-type Si for 30 minutes in a forming gas atmosphere at 700°C. Electrical contacts to the sample were made via gold wires fixed to the Al or Ag contacts with a silver conductive paste.

Lifetime measurements

Lifetime measurements were done using the MicroWave detected PhotoConductance Decay (μW-PCD) using an iodine-ethanol surface passivation. This passivation was preferably used instead of SiN_x, as in some experiments the hydrogen (H) from the Plasma Enhanced Chemical Vapour Deposition (PECVD) SiN_x seemed to passivate the bulk at the deposition temperatures of about 400°C.

RESULTS AND DISCUSSION

Hall-measurements

Results at room temperature

Table 2 summarises the results of the transport properties of the majority charge carriers from Hall-measurements at room temperature.

ingot	dopant	position	ρ [Ohmcm]	n or p [$10^{16}cm^{-3}$]	μ_H [$Vscm^{-2}$]
Cz ref.	P	M	5.0	0.085	1470
A	Sb	T	0.34	3.1	585
A	Sb	M	0.91	0.57	1198
A	Sb	B	1.28	0.38	1271
B	P	T	0.37	2.9	587
B	P	M	0.63	0.94	1043
B	P	B	0.59	0.89	1190
C	As	T	0.028	48	448
C	As	M	0.039	32	508
C	As	B	0.044	25	554
p ref.	B	T	1.4	1.7	267
p ref.	B	M	1.8	1.4	255
p ref.	B	B	1.7	1.2	301

Table 2: Transport properties of the majority charge carriers from Hall-measurements at room temperature from bottom (B), middle (M) and top (T) ingot position.

Samples were taken from each column from bottom

middle and top positions. For comparison, wafers from p-type (boron doped) ingot crystallised in a HEM furnace were characterisied as well. Figure 2 depicts the measured mobility as a function of the doping concentration in comparison with the theoretical limit.

The mobilities of the majority charge carriers are in the case of n-type Si from the B- and M-positions in the column very close to the theoretical limit, which is given mainly by scattering at acoustical phonons. Mobilities so close to the theoretical limit (>90% of the value in ideal monocrystalline silicon) have, to our knowledge, not been demonstrated for comparable p-type mc-Si wafers. Additional measurements on high quality p-type mc-Si material, as shown in Figure 2, support this statement. The doping concentration over the p-type column is more homogeneous but the mobility from all positions is, in the best case, 75% of the theoretical maximum. This means that other scattering mechanisms reduce the mobility in the case of p-type mc-Si material, but are not present in n-type mc-Si. Temperature dependent Hall-measurements were performed in order to identify the origin for this mobility decrease.

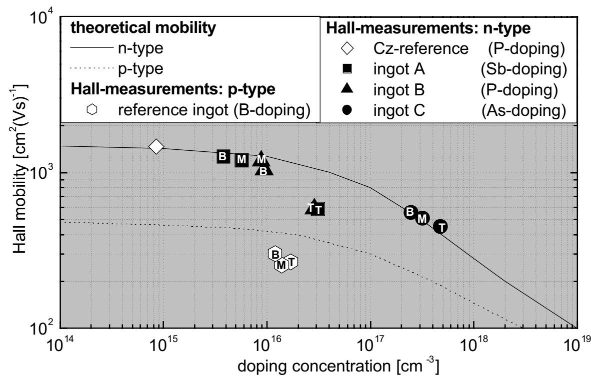

Figure 2: Hall mobilities of majority charge carriers at room temperature for three n-type ingots and one p-type ingot measured at bottom (B), middle (M) and top (T) positions in comparison with the theoretical limit.

Temperature dependent results

Figure 3 shows the temperature dependency of the corresponding Hall mobility. The mobility of the charge carriers from n-type mc-Si material grown into an experimental small ingot is depicted in the same figure. The mobility curves show typical temperature dependence according to equation (1) except for the wafer of a small, experimental ingot. This abnormality in mobility propagation can be explained by scattering of the electrons on a charged grain boundary [5]. This effect can be observed in rather low quality material and is in some cases reparable by H-passivation. In general, the mobility is dominated by different scattering mechanisms.

Looking at the temperature dependence, the scattering mechanism can be estimated from the exponent x in the formula

$$\mu \propto CT^{-x} \quad (1)$$

where T is the temperature, C a constant and x the scattering parameter. Theoretical calculations reveal that the mobility in non-polarised semiconductors (Si, Ge) is dominated by acoustic phonon interaction. The result is therefore expected to be proportional to $T^{-3/2}$.

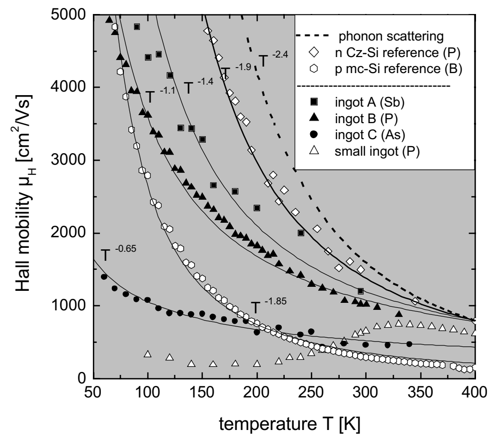

Figure 3: Temperature dependence of the Hall mobility.

Reported values for x are -2.4 for n-type and -2.2 for p-type mono-crystalline Si which could be due to an additional scattering at optical phonons. Doped Si also shows a different temperature dependency in the mobility curve because of an additional presence of charged scattering centres (doping atoms). The reason for the difference in the mobility between p-type and n-type Si remains unclear.

Lifetime measurements

Lifetime mapping was done on wafers from ingot A using µW-PCD method. The wafer surface was passivated by a 0.8 molar iodine/ethanol solution. A map of a wafer from a middle position of the column is shown in Figure 4.

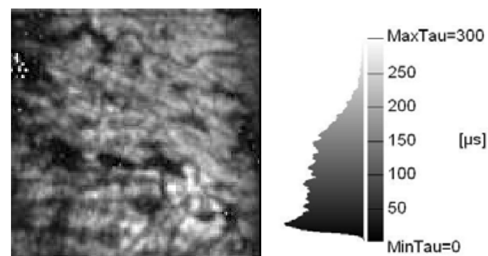

Figure 4: Lifetime mapping (τ_b = 122 µs) on cutout of 8 x 8 cm^2 from a 12.5 x 12.5 cm^2 mc-Si wafer.

The minority charge carriers show a very high bulk lifetime of 122 µs averaged over the entire wafer area. Gettering and H-passivation experiments have been done on Si-wafers from the experimental small ingot in the past and demonstrated that the initial lifetime could be increased by 150% [6].

Effect of boron diffusion on material properties

The temperatures used for boron diffusion in the electronic industry are usually above 1000°C, due to the lower diffusivity of boron compared to phosphorous. In addition, the boron diffusion was thought not to have a gettering effect, unlike phosphorous, which has been shown to partly compensate some degradation effects. Therefore, boron diffusion may be expected to degrade mc-Si.

We measured the bulk lifetime before (Figure 5a) and after BBr_3-diffusion in an open-tube furnace and removal of the doped region (Figure 5b).

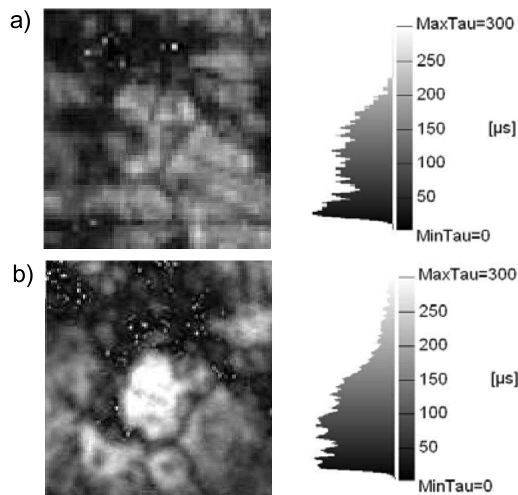

Figure 5: a) Initial lifetime mapping (τ_b = 95 µs) and b) lifetime mapping after boron-diffusion (τ_b = 108 µs, size of the measured wafers: 4 x 4.2 cm^2) [6].

The average lifetime remained nearly unchanged and some areas showed even higher lifetimes after the diffusion. Since such high temperatures without any gettering will certainly cause some degradation of multi-crystalline material, this is a strong indication of gettering by the boron-rich-layer that was present in our diffusion conditions. We suppose this to have a gettering effect on electrical defects/metallic impurities. This possible boron gettering of the n-type Si material will be presented in a forthcoming publication.

CONCLUSION AND OUTLOOK

We have demonstrated that the transport properties of majority charge carriers in directionally solidified n-type Si material are better than in p-type Si as mobilities so close to the theoretical value have, to our knowledge, not been demonstrated for comparable p-type mc-Si wafers. Temperature dependent measurements of the mobility did not explain this observation and therefore more experimental data is needed.

We note that the widely used QSSPC lifetime measurement has to make an assumption about mobilities to determine the carrier lifetime. If the values for monocrystalline silicon are used, as is probably often the case, the lifetime will be underestimated. Our results show that, if the mobility difference between n- and p-type silicon is similar for *minority* as it is for *majority* carriers, this underestimate may be stronger for p-type silicon than for n-type silicon. At least on our material, the n-type QSSPC lifetimes should be reasonably accurate, whereas the p-type QSSPC lifetimes would be underestimated by approx. 25%. Clearly, this causes some reduction of the observed lifetime differences between n- and p-type silicon.

Measurements on wafers with iodine/ethanol passivated surfaces using the µW-PCD method show exceptionally high bulk lifetimes of 122 µs averaged over a wafer area of 64 cm^2. Future experiments on these wafers will determine if the lifetimes can be increased to values of 300 µs, as expected.

The most questionable processing step within n-type solar cell production – the boron diffusion – was demonstrated not to have a degrading effect on the Si-material at the temperatures used. In contrast, the boron diffusion process seems to have a slight gettering effect. We therefore believe that we now have the means to demonstrate high efficiency solar cells on this n-type mc-Si material. An additional paper dealing with processing of n-type solar cells with B-emitter is submitted to this conference [1]. A back junction solar cell concept with industrially relevant processing techniques is also optimised on this material [7] leading to efficiencies of 14% on large area wafers of 156 cm^2 underlining the excellent quality of the Si material.

ACKNOWLEDGEMENTS

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