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REVIEW ON RIBBON SILICON TECHNIQUES FOR COST REDUCTION IN PV

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ABSTRACT

The shortage of Si feedstock and the goal of reducing W_p costs in photovoltaics (PV) is the driving force to look for alternatives to ingot grown multicrystalline (mc) Si wafers which have the highest share in the PV market. Ribbon Si seems to be a very promising candidate as no kerf losses occur, resulting in reduced Si costs per W_p. In addition, there is no need for the energy consuming crystallization of the ingot and therefore energy payback times can be significantly reduced.

The higher defect density in ribbon Si materials has to be taken into account during cell processing, but ribbon materials already commercially available show excellent efficiencies, while for the most promising techniques efficiencies are significantly lower, but very promising.

In this presentation an overview of ribbon Si technologies currently under research will be given, based on available data on crystal growth as well as solar cell processing and cell parameters.

INTRODUCTION

Ribbon Si wafers are a promising cost effective alternative to mc-Si wafers sliced from cast ingots as no kerf losses occur. These kerf losses together with contaminated parts near the edges of the ingot that cannot be used for cell processing add up to more than 50% of the Si starting material [1]. In addition, the current bottleneck in crystalline Si PV due to the shortage of Si feedstock increases Si prices and puts additional pressure on the fraction of wafer costs in the module.

A possible alternative to slicing wafers out of a crystallised ingot while maintaining the well proven processing techniques developed for mc-Si solar cells is the use of ribbon Si wafers. As no kerf losses occur and almost 100% of the Si feedstock ends up in the wafer material, a dramatic decrease in wafer costs is available. Apart from the better Si usage, energy costs are reduced as well, as time and energy-consuming ingot growth is eliminated. Therefore, a significantly reduced energy payback time for the PV module can be expected [2].

RIBBON SILICON CRYSTAL GROWTH TECHNIQUES

Ribbon Si crystal growth techniques can be distinguished by the shape of the meniscus that forms between the Si melt and the growing wafer [3], Fig. 1. While M_1 and M_2 are typical shapes for vertical ribbon growth methods, the large liquid/solid interface of M_3 normally occurs for horizontal growth techniques where a supporting substrate is used.

A typical example for the M_1 shape is EFG (Edge-defined Film-fed Growth) Si from Schott Solar, where the lower part of the meniscus is formed by a shaping element, a graphite die [4]. Tubes with octagon shape and facet widths of 12.5 cm can be grown.

Fig. 1: Shape of meniscus for different ribbon Si techniques.

Evergreen Solar's SR (String Ribbon) with a free meniscus base on top of the molten Si is an example of the M_2 geometry [5]. The advantage compared to EFG is the less restricted temperature control required near the liquid/solid interface (about 10 K instead of 1 K for EFG), which allows for a less complex furnace design. Strings that are fed through the molten Si provide edge support of the growing wafer. Throughput is lower compared to EFG as currently only two ribbons of 8 cm width are grown from one furnace (although the realisation of a four ribbon geometry is currently under investigation [6]). Both EFG and SR are already in industrial mass production.

The RGS (Ribbon Growth on Substrate) technique, currently under development at ECN, uses a substrate for support of the growing wafer and exhibits a M_3 meniscus shape [7]. This geometry enables a decoupling of directions of wafer pulling and crystallisation and therefore enables very fast growth speeds. The shape of the wafer is determined by the size of the casting frame and the sub-

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strate that is pulled underneath the frame with the molten Si in it (current width: 10 cm with a pilot line under construction aiming for 15.6 cm).

GE Energy's MW (Molded Wafer) technique (formerly called Silicon Film) uses a substrate (width 15.6 cm) and a high growth speed (300 cm/min) [8].

The RST (Ribbon on a Sacrificial Template) technique, formerly called RAD and now again under development at Solarforce, is characterised by a vertical growth direction combined with the use of a substrate [9]. This results in a faster growth speed as compared to EFG and SR. Thickness of the 10 cm wide ribbon will be 200 µm in the initial stage (5 cm/min) but is planned to be as low as 80 µm in the future (10 cm/min).

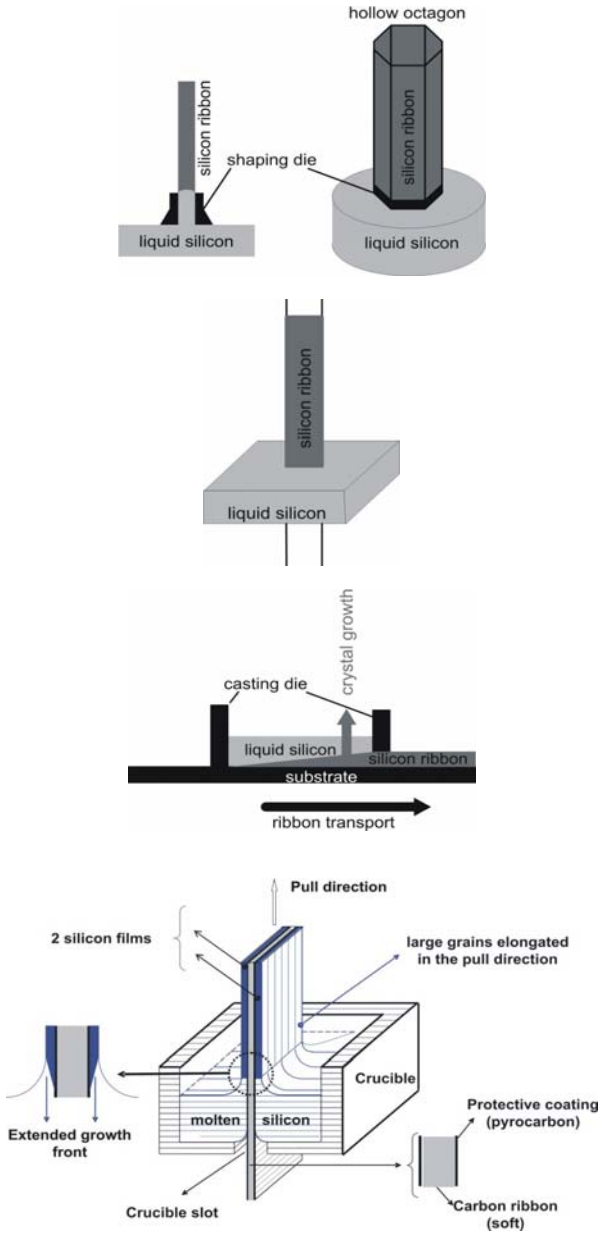

Fig. 2: Schematics of the ribbon Si techniques. From top to bottom: EFG, SR, RGS, RST.

Table 1: Properties of ribbon Si growth techniques.

	meniscus	pull speed [cm/min]	throughput [cm^2/min]
EFG	M_1	1-2	136
SR	M_2	1-2	13
RGS	M_3	650	6500 (10140)
MW	M_3	~300	4680
RST	M_2/M_3	5 (10)	100 (200)

DEFECTS IN RIBBON SILICON

Due to the specific growth condition, each ribbon technique results in different defect concentrations and distributions. It can be stated that there is a trend towards smaller grain sizes with increased pulling speed. EFG wafers tend to have a high [C] due to the graphite die close to the liquid/solid interface. Both EFG and SR show a low [O], and strong efforts led to a significant reduction in [O] for RGS, which is now in the range of ingot cast mc-Si. Nevertheless, RGS still has to deal with very high [C] at the moment. MW has to deal with both high [C] and high [O], while RST has similar properties as EFG.

Table 2: Interstitial oxygen and substitutional carbon content as well as grain size for ribbon Si materials.

	$[O_i]$ [10^{17} cm^{-3}]	$[C_s]$ [10^{17} cm^{-3}]	grain size
EFG	<1	10-15	cm^2
SR	<1	5-7	cm^2
RGS	3-5	20-30	<mm^2
MW	2-10	3-5	mm^2
RST	<1	5	mm^2-cm^2

GETTERING AND HYDROGENATION

To improve crystal quality and electronic properties of ribbon Si, gettering and hydrogenation techniques play a key role for reaching higher cell efficiencies [10]. They are normally part of solar cell processing in order to reduce cost while not applying additional processing steps. An exception is MW, where an annealing step is routinely carried out prior to cell processing which can significantly reduce interstitial O and substitutional C concentration in the upper part of the wafer [11], leading to fewer defects in the active area.

Several authors recently described gettering and hydrogenation studies in ribbon Si, especially for EFG, SR, and RGS, and strong improvements in carrier lifetimes have been observed [12-17]. Trapping of H in Si seems to be a crucial mechanism to explain the largely differing effective diffusion constant of H in Si. To a large degree this can be attributed to the O acting as a trapping centre for H, especially in precipitated form [18].

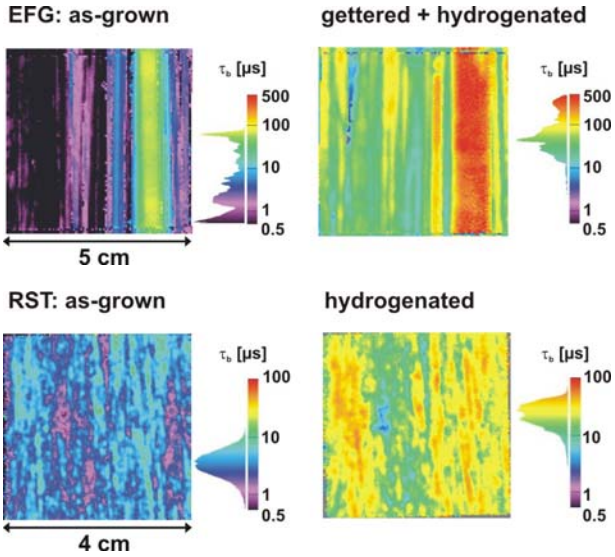

Fig. 3: Minority carrier bulk lifetimes of an EFG sample in the as-grown state and after gettering and hydrogenation using PECVD SiN_x deposition plus firing, top. RST sample as-grown and after hydrogenation using microwave-induced remote hydrogen plasma (MIRHP), bottom.

The distribution of metal impurities and other defects is different in ribbon materials compared to ingot cast wafers [19]. The precipitates present in ribbons after crystallization show a tendency to be smaller and more homogenously distributed because of the faster cooling rates, giving the impurities less time for precipitation [20].

SOLAR CELLS

To evaluate the potential of solar cells processed from ribbon Si materials, industrial-type and lab-type cell processes (Fig. 4) have to be distinguished. While the first one demonstrates the behaviour on large wafer formats with fabrication methods suitable for mass production, the latter is used for determination of the ultimate efficiency potential of a material.

Record cell efficiencies reached on ribbon Si wafers are shown in Table 3. Listed are record values for the corresponding materials and processes, to the best of our knowledge. There are no cell data available yet for RST material. Efficiencies in the 18% range are possible using lab-type processes on EFG and SR. These cells are mainly limited by recombination at the back side, where a full Al back surface field was applied, and a lack of an effective surface texture. Record cell efficiencies for industrial-type processes for these materials are in the 16% range. One reason for this discrepancy apart from process related issues is the inhomogeneous material quality causing lower efficiencies on larger cell formats.

Lab-type processing for RGS and MW using current material quality results in efficiencies in the 13-14% range, mainly limited by diffusion lengths of ~100 µm. Industrial cell processing leads to efficiencies of about 12-13%.

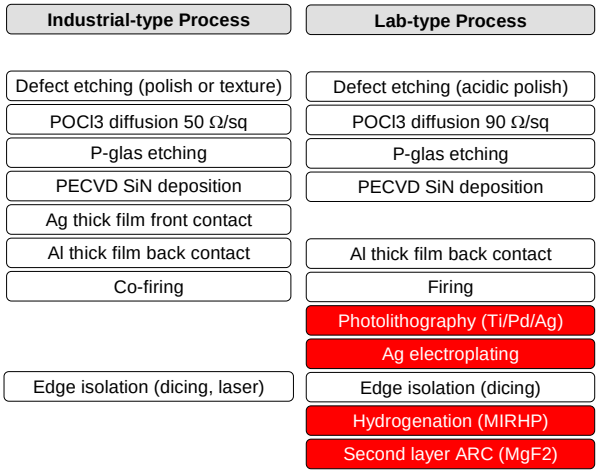

Fig. 4: Examples for an industrial (left) and a lab-type photolithography based cell process (right).

While EFG and SR are already comparable with standard ingot cast mc-Si efficiencies, RGS and MW still have to be improved in quality to reach higher efficiencies. If this can be achieved, a significant cost reduction in PV is possible, as the throughput of these materials is so high.

The application of a surface texture for minimizing optical losses is another issue to be addressed in the future. Due to the shiny surface of EFG and SR material without any surface damage, standard alkaline or acidic textures do not work well. Up to now there are no reports of increased cell efficiency for textured EFG or SR. RGS and MW material behave differently, as an acidic surface texture has already been demonstrated [15, 21].

Table 3: Cell parameters of record cells for different ribbon technologies. L: lab-type, I: industrial-type process.

Material	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
EFG L 4 cm^2 [22]	624	36.8	79.2	18.2
EFG I 100 cm^2 [23]	603	33.4	78.7	15.7
SR L 4 cm^2 [22]	621	36.7	78.6	17.9
SR I 80 cm^2 [24]	609	33.8	77.6	16.0
RGS L 4 cm^2	587	29.2	78.0	13.4
RGS I 25 cm^2 [15]	589	28.6	76.3	12.9
MW L 4 cm^2	570	31.4	78.0	14.0
MW I 25 cm^2 [21]	559	28.5	75.0	11.9

SI USAGE AND ENERGY PAY-BACK TIME

An interesting measure in PV today with the predicted Si shortage becoming a reality is the amount of Si feedstock that is used to generate 1 W_p of power. Under the simplified assumption that 100% of the feedstock ends up in the wafers for all ribbon techniques, this g/W_p (or t/MW_p) data can be calculated with wafer dimensions and record efficiencies for industrial-type cell process as input parameters for a rough estimate (Table 4, no efficiencies available for RST). For mc-Si an average efficiency value of 15% is assumed. A significant reduction in Si feedstock

per generated W_p can be achieved when using ribbon Si techniques. For MW more impurities in the Si feedstock can be tolerated, therefore feedstock costs are significantly lower than for standard mc-Si ingot wafers as well.

Apart from lower Si feedstock consumption, avoidance of time and energy consuming ingot crystallization steps brings down wafer costs for ribbon techniques as well. This results in a significantly reduced energy payback time of the ribbon Si solar module, provided module efficiencies are high enough, as shown e.g. in [2].

Table 4: Si feedstock usage per generated W_p.
*: photolithography process, first test
**: no standard electronic grade Si needed

Material	**thickness [µm]**	**η [%]**	**g_{Si}/W_p**
mc-Si ingot	~250	15	10.5
EFG	300	16	4.4
SR	300	16	4.4
RGS	300*(150)*	13*(11*)*	5.4*(3.2)*
MW	600	12*(14*)*	11.7*(10.1)***

SUMMARY

Ribbon Si technologies can be distinguished by the shape of the meniscus at the liquid/solid interface. By this approach the classical vertical growth techniques EFG and SR with lower pulling speeds (1-2 cm/min) can be separated from the horizontal growth techniques RGS and MW with higher pulling speeds (300-650 cm/min), allowing a higher throughput. RST can be classified as a mixture of these two classes.

The higher defect density in ribbon Si as compared to standard mc-Si from ingots can be addressed by optimised gettering and hydrogenation schemes. Due to the fast crystallization and varying impurity concentrations, the distribution and size of precipitates present in ribbons can differ significantly from ingot grown mc-Si material.

In EFG and SR excellent lifetimes can be reached with record cell efficiencies in the same range as for mc-Si from ingots, although some extended lower quality areas still limit cell performance [25].

For RGS and MW gettering and hydrogenation are very important process steps, too, but the higher defect density and the lower as-grown crystal quality is still limiting cell efficiencies.

The Si feedstock usage per W_p can be reduced, and in combination with lower energy consumption during crystallization, energy payback times can be shortened. All this should lead to a significant reduction in W_p costs.

Data published on Sharp's ribbon technique (M_3 meniscus, similar to RGS) is very limited, therefore it was not included in this overview.

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