ANALYSIS OF PROCESSING STEPS FOR INDUSTRIAL LARGE AREA n-TYPE SOLAR CELLS WITH SCREEN PRINTED ALUMINUM-ALLOYED REAR EMITTER AND SELECTIVE FSF

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ABSTRACT: Applying the standard process for p-type solar cells to n-type silicon results in a “PhosTop” solar cell with a screen printed alloyed aluminum emitter on the rear side [1]. This cell concept can be improved by adding a selective FSF and a SiO_2/PECVD SiN_x stack passivation layer, resulting in a highest confirmed stable efficiency of 19.4 % for 6” n-type Cz-Si solar cells [2]. Besides a very low front SRV, this cell concept also demands for a very high bulk lifetime. We therefore analyze the change of bulk lifetime and conductivity after each high temperature process step in the applied cell process. Furthermore we investigate the current generation from the unprinted wafer edge with no emitter.
Keywords: n-type, silicon, lifetime

1 INTRODUCTION

The standard processing sequence for p-type monocrystalline silicon (including screen printed metallization fired through a SiN_x ARC and a full Al back surface field) has been well optimized for many years leading to solar cell efficiencies up to 19.2 % [3].

The progress in Al paste development as well as application of a selective emitter makes the base lifetime a significant limitation for the cell efficiency.

Using n-type silicon instead of p-type offers a much higher minority carrier lifetime since due to the absence of boron, there is no light-induced degradation [4]. Furthermore, n-type silicon is more tolerant to metal impurities [5]. If the same processing sequence is applied to n-type Cz silicon, a rear junction solar cell with a phosphorous front surface fields is formed [1].

Since for a rear junction solar cell most of the charge carriers are still generated close to the front surface, this cell type requires a very high bulk lifetime and front surface passivation quality. The PC1D simulation shown in Fig. 1 illustrates, that a bulk minority charge carrier lifetime larger than approx. 4 ms is required for a cell thickness of 175 µm if the loss in cell efficiency due to bulk recombination should be less than 0.1 $\%_{abs}$.

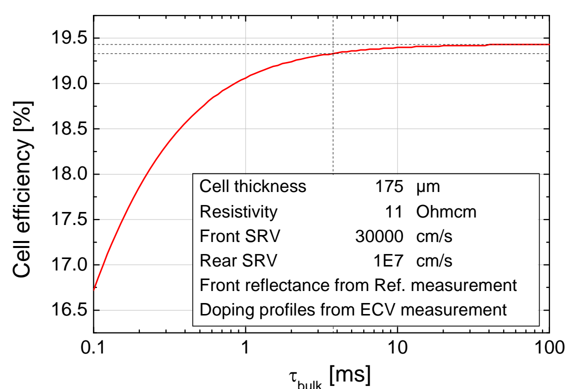

Figure 1: PC1D simulation of the cell efficiency vs. base minority carrier lifetime for an n-type rear emitter solar cell.

2 SOLAR CELL PROCESSING SEQUENCE

The processing sequence used to create the n-type rear junction solar cells is based on the standard screen-printing process for p-type solar cells which is widely used in industrial production. It starts with an alkaline random pyramid texture and a 35 Ω/□ $POCl_3$ diffusion, the edge isolation is carried out by single side etching. For a selective FSF, the front surface hast to be masked by inkjet- or screen-printing in the area that will be contacted. The FSF is then etched back in an acidic solution to the desired sheet resistance (compare [2,3,6]). If the front surface is passivated by a SiO_2/SiN_x-stack, a RCA clean is performed followed by a dry thermal oxidation resulting in an approx. 10 nm thick SiO_2 layer on the front side. The subsequent process steps remain unchanged from the standard p-type solar cell process, which continues with the plasma-enhanced chemical vapor deposition (PECVD) of SiN_x (direct plasma, low frequency), aligned screen printing of the metallization and co-firing.

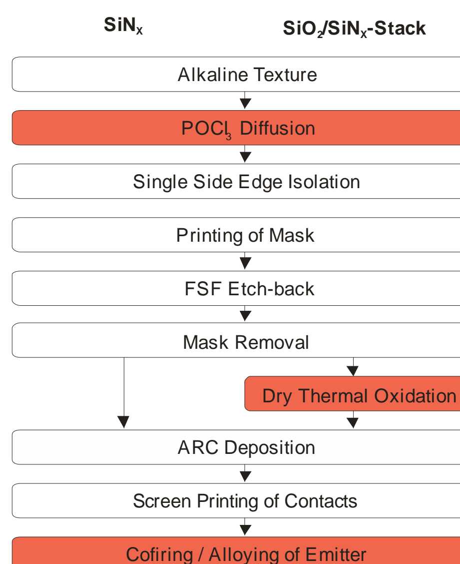

Figure 2: Processing sequence to create a rear Al emitter solar cell with a selective FSF and a SiN_x (left) or SiO_2/SiN_x-stack (right) front side passivation. The high temperature processing steps are marked in red.

3 EXPERIMENTAL

In this work we present a bulk lifetime monitoring for the high temperature process steps included in the described processing sequence. Furthermore we investigate the current collection from the unprinted wafer edge at the rear side of the cell that is not covered by an emitter.

3.1. Influence of processing steps on the bulk lifetime

To determine the influence of each high temperature step on the resistivity and lifetime of the bulk silicon, three groups of lifetime samples were processed taking them out of the process:

- as cut (alkaline texture)
- after $POCl_3$ diffusion (alkaline texture, HCl/HF clean, 35 Ω/□ diffusion)
- after SiN_x (alkaline texture, HCl/HF clean, 35 Ω/□ diffusion, PECVD-SiN_x:H, firing, removal of SiN_x)

We have investigated three different n-type Cz-Si substrates (A-C) and two p-type Cz-Si substrates (D,E) from different suppliers.

3.2 Sample preparation

After being exposed to the investigated process steps, the samples were chemically polish etched to remove the surface (9 µm per side) and were cleaned in piranha solution. Finally both sides were passivated by an approx. 60 nm thick intrinsic amorphous silicon (a-Si:H) layer deposited at a set temperature of 225 °C in a direct plasma enhanced chemical vapor deposition (PECVD) reactor. After the deposition, all samples were thermally annealed at a set temperature of 320 °C for 16 min under N_2 atmosphere to activate the surface passivation.

4 RESULTS

4.1. Effective lifetime and resistivity

On all samples photo conductance decay (PCD) measurements were performed using a Sinton WCT-120 lifetime tester. The effective minority carrier lifetime at a minority carrier density of $1\cdot10^{15}$ cm^{-3} and the resistivity are shown in Fig. 3-5.

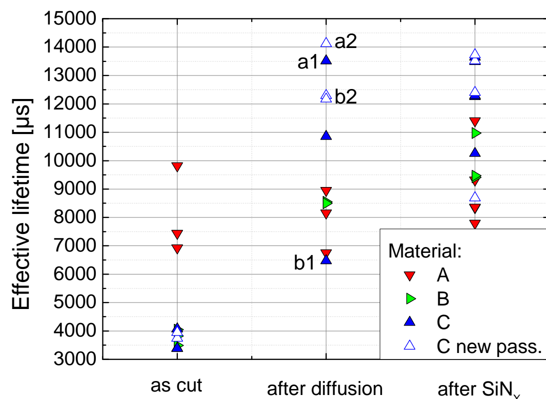

Figure 3: Effective lifetime of the **n-type** substrates at a minority carrier density of $1\cdot10^{15}$ cm^{-3} measured by the PCD method. The letters in the graph indicate lifetime values of the samples shown in Fig. 6.

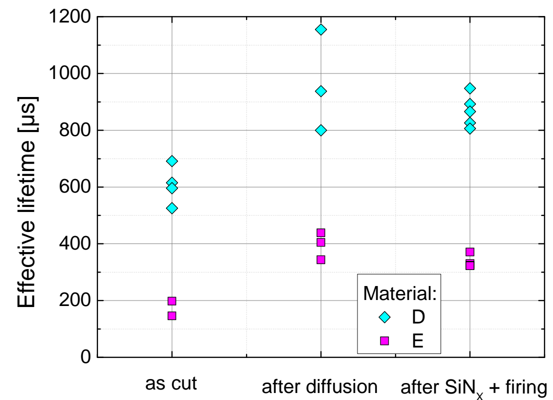

Figure 4: Effective lifetime of the **p-type** substrates at a minority carrier density of $1\cdot10^{15}$ cm^{-3}

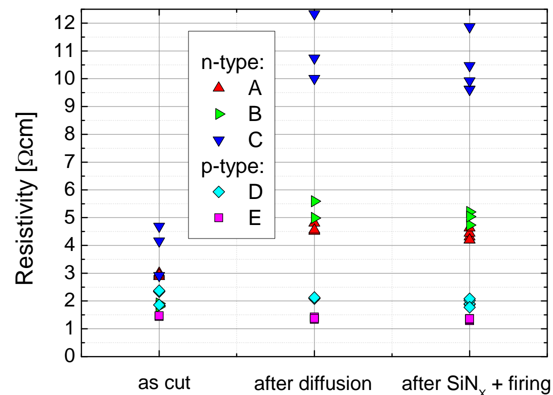

Figure 5: Resistivity of the n- and p-type substrates measured by the PCD method

On all substrates, the measurements show a strong increase in bulk lifetime after the $POCl_3$ diffusion. The resistivity increases on n-type- and decreases on p-type substrates. Both resistivity effects are most probably caused by the annihilation of thermal donors in the bulk silicon which act as double donors [7-9], while the lifetime behavior is also affected by the gettering effect of the $POCl_3$ diffusion. The very high lifetimes measured on the n-type substrates after the process can be regarded as a lower limit for the bulk lifetime of the finished solar cell, however the high variation in effective lifetime of equally processed samples makes it difficult to draw any further conclusions from this data.

Photoluminescence (PL) images of the samples show that the variation is caused by strong spatial inhomogeneities (see Fig. 6 top). In order to distinguish whether the inhomogeneities in the PL images are caused by the passivation quality or by the bulk lifetime, the passivation layer and the Si surface (approx. 3 µm) of the samples from material C were removed in 23 % KOH at 80 °C and the samples were passivated again by an a-Si:H layer. The PL images after the new passivation (Fig. 6 bottom) show no similarity to the ones before, proving that the inhomogeneities are not caused by the bulk material but by the a-Si passivation layer.

The lifetimes measured after the new passivation are indicated by the empty blue symbols in Fig. 3.

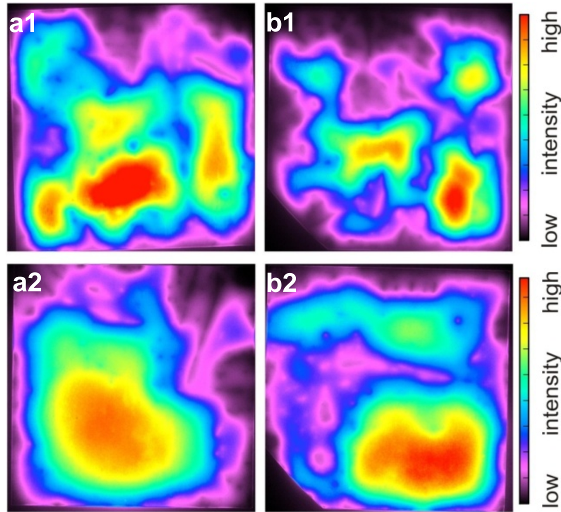

Figure 6: PL images (linear scale) of two equally processed samples from substrate C after the diffusion with the highest (top left) and lowest (top right) minority carrier lifetime. The bottom images show the same samples after a new passivation.

The same experiment was repeated later only with substrate A to evaluate the influence of the dry thermal oxidation. The samples were exposed to a 30 Ω/□ diffusion and an etch-back to approx. 100 Ω/□. Subsequently one group of samples was cleaned in piranha solution and exposed to a dry thermal oxidation at 900 °C for 5 min, the other group remained as a reference. All samples were then chemically polish etched and passivated as described in section 3.1.1. The lifetime results are illustrated in Fig. 7. Although a slight decrease of average lifetimes might be observable, the conclusion is that the thermal oxidation does not harm the bulk material quality significantly.

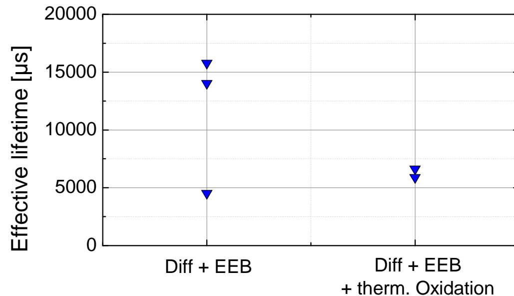

Figure 7: Effective lifetime before and after a thermal oxidation, evaluated at a minority carrier density of $1 \cdot 10^{15}$ cm^{-3}.

4.2. Current collection at the unprinted cell edge

On the solar cell rear side the aluminum emitter cannot be printed over the full area, the unprinted area therefore has no emitter (in our case approx. 1 mm wide). Minority charge carriers generated in the unprinted area need to reach the emitter by diffusion. However, the effective diffusion length is short since the rear side is not passivated. Furthermore, the diffusion of charge carriers generated above the emitter towards the unpassivated rear side leads to losses in the quantum efficiency close the emitter edge. Both effects can be observed in an 833 nm LBIC (Light Beam Induced Current) linescan over the cell edge of an Al rear emitter solar cell (see red line in Fig. 8). If the unprinted edge is removed, the decay in EQE (External Quantum Efficiency) towards the cell edge is even steeper (blue line) since the unpassivated edge is now vertical. This leads to a loss in total current (red dashed area), but an increase in current density.

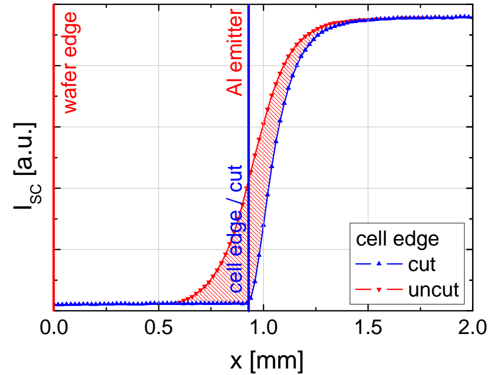

Figure 8: 833 nm LBIC linescan over the wafer edge of a rear Al emitter solar cell before (red) and after (blue) removing the unprinted cell edge.

4.3. Solar cell results

We have processed solar cells from n-type Cz-Si wafers according to the described processing in Fig. 1, the results have been published in [2] and are shown in Table I. All measurements were performed at UKN, the efficiency of the best solar cell was confirmed by Fraunhofer ISE Callab to 19.4 %.

Table I: IV measurement results of 6” Cz-Si n-type solar cells (substrate C) with a rear Al emitter after removing the unprinted wafer edge [6]. The average values are taken from 4-6 cells.

Front side passivation	FF [%]	V_{OC} [mV]	j_{SC} [mA/cm^2]	η [%]
SiN_x	79.5	641	37.1	18.9
$SiO_2 + SiN_x$	79.8	649	37.5	19.4

On 5” p-type silicon (material D), the same processes have lead to a V_{oc} of 641 mV (SiN_x) and 650 mV (SiO_2 + SiN_x). Due to the different cell size and grid design, the complete IV data is not directly comparable with the n-type cells.

5 CONCLUSION

The effect of the high temperature processing steps included in the processing sequence for Al rear junction solar cells was investigated by measuring the effective lifetime and bulk resistivity of symmetrical samples passivated by a thin a-Si:H layer.

On n-type silicon, a strong increase in bulk lifetime and resistivity was observed, which could be caused by the annihilation of thermal donors during the diffusion step. This has to be considered when designing the solar cell process for these types of rear emitter solar cells. The effective lifetime of equally processed samples varied strongly due to spatial inhomogeneities in the surface passivation quality. However, for all substrates effective

lifetimes larger than 8 ms were measured after the process.

Using 6” n-type Cz silicon, the investigated solar cell process has resulted in a highest independently confirmed efficiency of 19.4 % on a screen printed full area Al emitter solar cell.

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