SIMPLE MINI MODULE FABRICATION SCHEMES FOR HIGH VOLTAGE SILICON SOLAR CELLS

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ABSTRACT: State of the art crystalline silicon back contact solar cell concepts like the EWT (emitter wrap through) and the MWT/MWA (metallisation wrap through/around) approach have the potential to simplify cell connection and module fabrication. Additionally they can also be used in small area monolithically integrated solar cells as well as quasi-monolithic mini modules designed for mobile consumer product applications. In this work two different concepts for mini modules of back contact solar cells are presented and discussed: The MWT/EWT-type "HighVo" solar cell and a substrate-based quasi-monolithic series connection. First experimental results for prototypes of these concepts are: MWT-HighVo solar cells with a conversion efficiency η of 12.8 % and an open circuit voltage V_{oc} of 3.5 V; EWT-HighVo solar cells with η = 10.6 % and V_{oc} = 5.58 V, quasi-monolithic series connected solar cells with η = 11.3 % and V_{oc} = 8.18 V.
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1. INTRODUCTION

The increasing number of power intensive mobile consumer and telecommunication electronics represent a new and interesting market for solar cell mini modules. Important prerequisites to access this market are output voltages of several volts, efficiencies well above the present predominant amorphous silicon thin film solar cell arrays, a sufficient device performance at low illumination intensities and - not to be underrated - a highly esthetic appearance of the device.

Existing attempts to achieve this goal are mini modules of shingled high efficiency crystalline silicon (c-Si) solar cells combined with small sized state of the art converter electronics [1] and monolithically integrated thin film modules. We propose alternative approaches based on standard low cost c-Si production techniques which revive the old idea of a non thin film monolithically series connected c-Si solar cell. These "high voltage" solar cells may have the potential to reach efficiencies as well as production costs in between the above mentioned high efficiency and thin film solutions.

2. THE SERIES CONNECTION CONCEPTS

2.1 The MWT "HighVo" Solar Cell Concept

A schematic drawing of the MWT [2] HighVo solar cell concept [3] is given in Fig.1. The basic features are:
- The existence of several unit cells (UC) defined by discrete emitter (2) and back contact regions (5) on one wafer (1) realized with the help of a SiN or screen printable diffusion mask.
- A partial isolation of UCs by inserting trenches (4) reaching from the cell front surface to the back surface whereby remaining narrow bridges guarantee the integrity of the device.

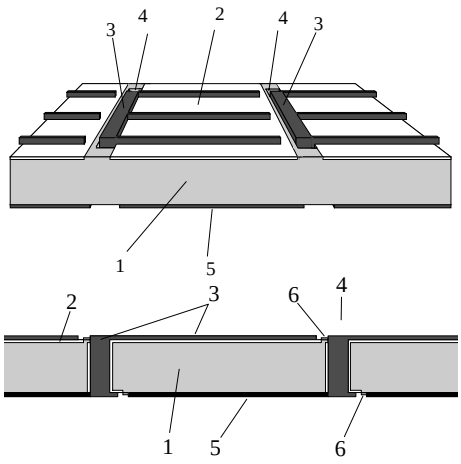

Figure 1: Sketch of one unit cell and parts of the neighboring unit cells of a MWT HighVo solar cell in top/side and cross sectional view. 1: silicon wafer, 2: emitter, 3: emitter contact, 4: isolation trench, 5: base contact, 6: diffusion barrier (not shown in upper drawing).

- A screen printed series connection: The series connection of neighboring UCs can be achieved by printing the emitter metallization (3) through the isolation trench (4) to contact the base metallization (5) of the neighboring UC. A shortening of the UCs themselves is circumvented by the emitter which also reaches via the trenches from the front to the backside. Additionally, the filling of the trenches recovers some of the original stability of the wafer.

The process sequence for the fabrication of prototypes of these cells was:
- saw damage removal
- formation of a diffusion mask on both sides of the wafer (SiN deposition, screen printing of an etch resist, plasma etching)
- formation of the isolation trenches with a dicing saw or a Nd/YAG laser
- short saw/laser damage etch
- $POCl_3$ emitter diffusion (30 Ω/sq.)

- screen printing of front and back contact plus co-firing
- single layer SiN antireflection coating (ARC) or ZnS / MgF_2 double layer antireflection coating (DARC) deposition

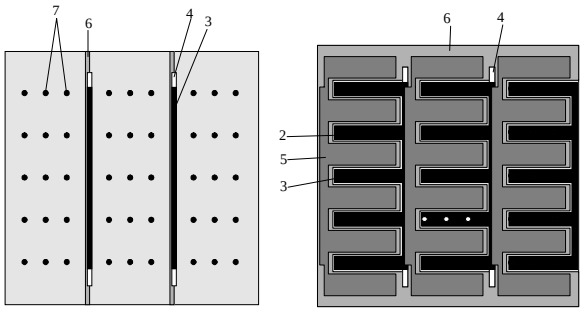

Figure 2: Front (left) and backside view (right) of an EWT-HighVo solar cell. 2: emitter, 3: emitter contact, 4: isolation trench, 5: base contact, 6: diffusion barrier, 7: holes. The white dots in the lower sketch symbolize the holes lying underneath the emitter contact metallization.

2.2 The EWT "HighVo" Solar Cell Concept

The isolation and series connection of UCs within this concept are realized in the same manner as described in 1.1 with some adjustments to obtain EWT-type UCs.

Fig. 2 presents the basic design of an EWT-HighVo solar cell with three UCs. Front and backside emitter (2) of the UCs are connected through many small holes (7). Cell emitter and base are contacted by an interdigitated finger grid (3,5). Again the isolation trenches (4) are covered by the emitter of the UCs. The emitter busbar of one UC is printed across the isolation trench to connect to the base metallization of the neighboring UC. Filling the trenches stabilizes the device.

The basic process sequence is the same as in the case of MWT-HighVo cells. The additional laser drilling of the holes has been performed together with the laser cutting of the isolation trench within one step.

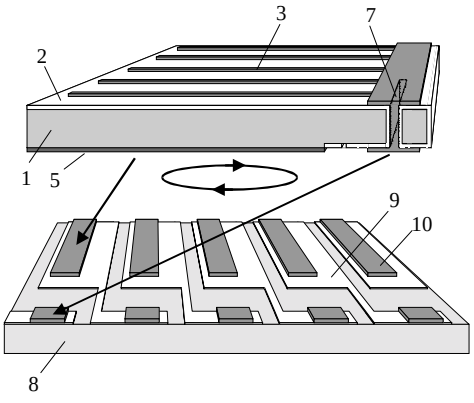

Figure 3: Schematic drawing of an MWT-type large area solar cell and a circuitry substrate which can be used for the fabrication of a "quasi-monolithic" series connection of small area unit cells produced on one wafer. 1-7: see Fig. 1 and 2, 8: substrate, 9: circuitry, 10: solder or conductive adhesive.

2.3 The "Quasi-Monolithic" Series Connection

Part of the basic idea of back contact cells is the simplification of the cell connection by using circuitry substrates [4]. This approach can easily be used for the fabrication of "quasi-monolithic" high voltage solar cell arrays if a large area back contact cell (e.g. 10 x 10 cm^2 or 15 x 15 cm^2) is cut into UCs after it has been fixed onto a circuitry substrate which ensures the series connection.

Fig. 3 illustrates the principle when an MWT-type solar cell (1) is used. The substrate (8) is covered by a circuitry (9) which defines the geometry of the UCs. The circuitry connects the base metallization (5) of the UCs with the emitter metallization (3) of the neighboring UCs. When fixing the cell onto the substrate it will be lying above the circuitry by a distance given by the thickness of the solder or conductive adhesive (10). This distance enables the separation of the cell in small UCs by means of a conventional wafer dicing saw in the last process step.

3. THEORETICAL ASPECTS

One consequence of our and of most other known concepts for non thin film monolithically integrated c-Si solar cells is the imperfect insulation between the UCs. The conductive wafer is the base of all UCs leading to parasitic current paths which bypass most of the pn-junctions of the UCs. These current paths are equivalent to additional shunting resistances lying in parallel to the ordinary shunt resistance of the pn-junctions. This results in a lowered over all shunt resistance R_{sheff} of the UCs with its distinct influence on cell performance especially at low illumination intensity levels. A detailed discussion of an appropriate equivalent circuit model [5] and simulations for various illumination levels, R_ps and UC numbers are given in [3]. The challenge in fabricating HighVo solar cells is therefore not only to achieve conversion efficiencies comparable to series connected ordinary screen printed c-Si solar cells but also to obtain comparable values for R_{sheff}.

In our concept the additional shunt resistance is determined by the geometry of the bridges holding the device together and the specific resistance ρ of the wafer. Therefore the bridges have to be prevented from a highly conductive emitter or contact region. The larger this region and ρ the larger R_{sheff}. This means that for the sake of a device performance at low intensities comparable to standard cells we have to sacrifice some carrier collecting emitter area and voltage which could be obtained on material of lower resistivity.

For the MWT-HighVo prototypes the distance between highly conductive layers of neighboring UCs respectively across the bridges has been kept at 2mm. For the prototypes of the EWT-HighVo cell the distance has been enlarged to 5mm. Another prototype of an EWT-HighVo cell has been fabricated with a meander shaped isolation trench (see Fig. 5). Within this meander concept the UCs are held by a non carrier collecting frame of wafer material. The distance between UCs across the bridges is now given by the width of the UCs further improving R_{sheff}. A meander shaped insulation trench leads to a more complex equivalent circuit model resulting in a series connection of non identical UCs which can be classified according to the symmetry in the circuit [6].

4. RESULTS

4.1. MWT-HighVo Solar Cells

MWT-HighVo cells were the first HighVo cells which we fabricated. Their geometry with 6 UCs and a total area of 21.07 cm^2 has been chosen predominantly for convenience and is not optimized for a certain application; only the UC area is kept roughly at a size which could be used for example in mobile telephone applications.

Fig. 4 shows a photograph of a MWT-HighVo cell (left) and the result of a lock-in thermography of an early stage HighVo cell (right). The shunting currents along the wafer bridges with their highest densities at the edges of the emitter and back contact layers of each UC are clearly visible. The bright spot in the lower left corner of the first UC is an ordinary shunt at a broken wafer edge. This thermogram proves that the MWT-type series connection does not generate any shunts in the isolation trench region. R_{sheff} of the UCs of the investigated HighVo cell is estimated to be about 350 Ωcm^2.

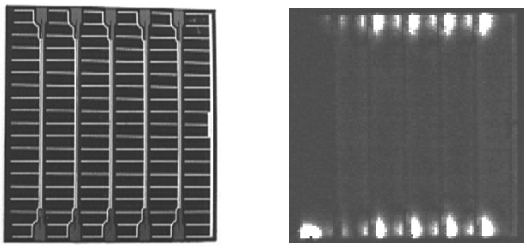

Figure 4: Photograph of an MWT-HighVo cell (left) and the result of a lock-in thermography measurement (right). The shunting currents along the wafer bridges with their highest densities at the edges of the emitter and back contact layers are clearly visible. The bright spot in the lower left corner is an ordinary shunt at a broken edge.

Table I: Performance parameters of the best MWT-HighVo devices - each with a total area of 21.07 cm^2 and 6 UCs - obtained under standard reporting conditions

best cells	**FF [%]**	**I_{SC} [mA]**	**V_{OC} [V]**	**V_{MPP} [V]**	**V_{OC} UC [mV]**	**J_{SC} UC [mA/cm²]**	**η [%]**
	69.4	75.4	3.44	*2.8*	574	21.5	*8.5*
ARC	70.2	99.7	3.45	*2.8*	575	28.4	*11.4*
DARC	71.6	107.9	3.50	*2.85*	583	30.7	*12.8*

With the same design we obtained MWT-HighVo cells with η = 12.8 %, a voltage at the maximum power point V_{mpp} = 2.8 V, V_{oc} = 3.45 V and $R_{sheff} \approx 500\ \Omega cm^2$. The results of the IV-measurements of the best cells are summarized in Table I. For the dependence of the cell performance on the illumination intensity see Fig. 6.

4.2. EWT-HighVo Solar Cells

Within the further cell development we increased R_{sheff} by enlarging the emitter free regions or by using the meander shaped isolation trench respectively the frame design as mentioned in section 3. At the same time the esthetical appearance of the HighVo cells has been improved by choosing an EWT design for the UCs. We fabricated EWT-HighVo cells with 3 UCs and a total area of 15.68 cm^2 (enlarged bridges, 5 mm) as well as EWT-HighVo cells in the frame design with 10 UCs, a total area of 40.32 cm^2 and an effective cell area of 35.72 cm^2. The latter cell is shown in Fig. 5.

The results of the IV-measurements of three of these solar cells are given in Table II. Cell EWT1 is a 3 UC device, cell EWT2 (EWT3) a 10 UC device in the frame design without (with) ARC. For a better comparison of the different devices and because the frame is supposed to be covered by an aperture within the application the performance parameters for the total and effective cell area of EWT2 and EWT3 are given. EWT2 has been measured with and without a somewhat imprecise shading mask. For EWT3 only calculated values are given.

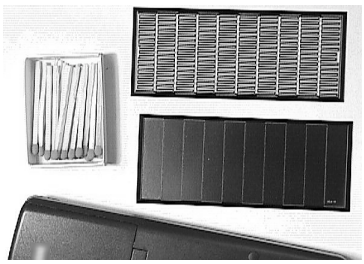

Figure 5: Photograph of the front and backside of an EWT-HighVo cell together with a mobile telephone.

The cells suffer from a reduction in V_{oc} of about 20 mV compared to the MWT-type cells which is mainly caused by an insufficient passivation of the enlarged pn-junction bordering the back surface. Additionally the fill factor is also affected by a high series resistance (see Fig. 6). The loss in front emitter due to the enlarged emitter free areas around the bridges could be compensated - resp. overcompensated in the case of EWT1 - by the reduction of shading losses. Therefore the conversion efficiency of the EWT-HighVo cells is quite close to the one of the MWT-type cells.

The most important improvement achieved by the new design is clearly visible in Fig. 6 which shows the dependence of the cell performance on the illumination intensity. Below an intensity of 22 mW/cm^2 EWT3 shows a higher conversion efficiency than the best MWT-type cell with DARC. The effective shunt resistance of the UCs of EWT3 is estimated to be about 2000 Ωcm^2 which is comparable to standard screen printed Si solar cells.

Future improvement in the cell performance can be expected from an optimized contact geometry of the UCs which should reduce the series resistance and an electronic passivation of both surfaces.

4.3. "Quasi-Monolithic" Series Connection

First prototypes have been fabricated to test the fixing of the cells on the substrate as well as the cutting of the cells on the substrate with a wafer dicing saw. The prototypes have been 10x10 cm^2 multi crystalline (mc) MWT solar cells with two busbars at the wafer edges and a standard finger spacing of 2.5 mm. The front of the MWT cell and the circuitry substrate are shown in Fig. 7.

Table II: IV-results of three EWT-HighVo solar cells under standard reporting conditions. Cell EWT2 has been measured with and without a shading mask. The effective area values for cell EWT3 are calculated.

parameter	EWT1, no ARC	EWT2, Frame, no ARC		EWT3, Frame, ARC
		total	masked	
total area [cm^2]	15.68	40.32	--	40.32
aperture [cm^2]	--	35.72	35.72	35.72
no. UCs	3	10	10	10
FF [%]	68.5	68.1	68.3	67.1
I_{sc} [mA]	117.3	81.6	80.4	113.7
V_{oc} [V]	1.66	5.48	5.48	5.58
V_{oc} UC [mV]	553	548	548	558
V_{mpp} [V]	1.29	4.28	4.26	4.30
J_{sc} UC [mA/cm^2]	22.4	20.2	22.5	28.2
J_{sc} UC aperture cal. [mA/cm^2]	22.4	22.8	22.5	31.8
η [%]	8.5	7.6	8.4	10.6
η apert. cal. [%]	8.5	8.5	8.4	11.9

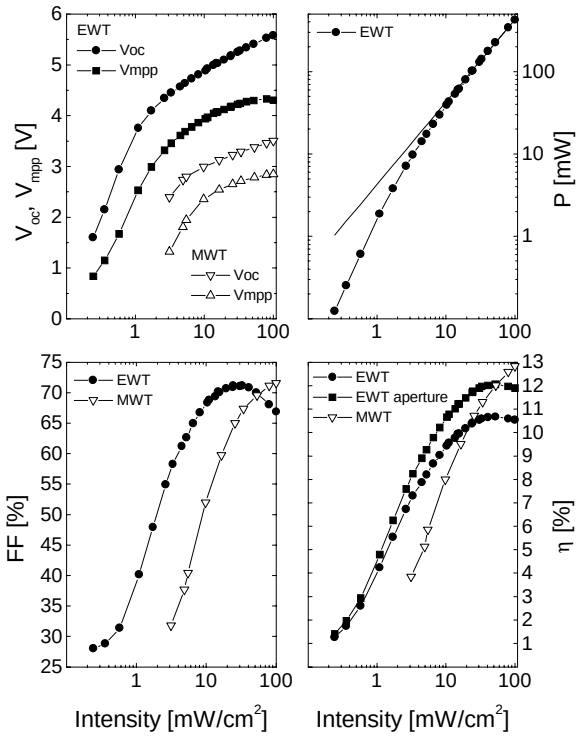

Figure 6: Dependence of the performance parameter on illumination intensity for cell EWT3 and a MWT-type HighVo cell. The better conversion efficiency of EWT3 at low intensities reflects the improvement in R_{sheff}. The maximum in FF indicates a high series resistance.

After having been fixed with a conductive adhesive the cells were cut into UCs of 10 x 0.7 cm^2. The IV-results of two mini modules together with a standard reference cell which has been fabricated within the same process are given in Table III. In principle the technique proved to be applicable although the efficiency of the prototypes is about 1 % absolute lower than the one of the standard cell. The main loss mechanism is the series resistance within the MWT cell itself. Besides the cell design the adhesive technique has to be further investigated and more reliable temperature cycle and climate tests have to be performed.

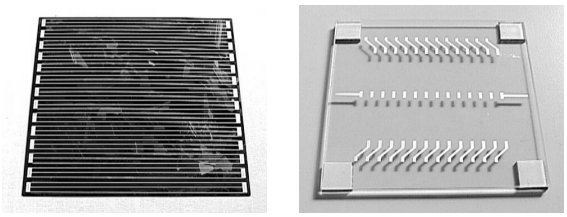

Figure 7: 10x10 cm^2 MWT solar cell and circuitry substrate which were used for testing the cell substrate connection and unit cell separation.

Table III: IV-results of quasi-monolithic substrate based mini modules compared to a standard cell fabricated within the same process.

parameter	ref. Cell	Sub1	Sub2
area [cm^2]	96.04	91	98
number UCs	1	13	14
FF [%]	76.7	72.6	69.1
I_{sc} [A]	2.663	0.189	0.196
J_{sc} UC [mA/cm^2]	27.7	27	28
V_{oc} [V]	0.593	7.66	8.18
Voc UC [mV]	593	589	584
V_{mpp} [V]	0.483	6.11	6.30
η [%]	12.6	11.6	11.3

5 CONCLUSION

Three new types of mini modules have been presented: MWT-HighVo cells (η = 12.8 %, V_{oc} = 3.5 V), EWT-HighVo cells (η = 10.6 %, V_{oc} = 5.58 V) and a circuitry substrate based series connection (η = 11.3 %, V_{oc} = 8.18 V). By sacrificing some carrier collecting emitter area a performance at low illumination intensity comparable to standard industrial type Si solar cells could be achieved. First experiments with a circuitry substrate based series connection were promising but the overall feasibility of this approach still has to be demonstrated e.g. cost effective and reliable adhesive techniques have to be developed.

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