OVER 14% EFFICIENCY ON RST-RIBBON SOLAR CELLS

P. Keller[1], U. Hess[1], S. Seren[1], J. Junge[1], F. de Moro[2], G. Hahn[1]
[1] University of Konstanz, Department of Physics, Jacob-Burckhardt-Str. 29, 78457 Konstanz, Germany
[2] Solarforce, 1 rue du Dauphin, 38300 Bourgoin-Jallieu, France

ABSTRACT: In solar cell production silicon wafer material still has a large impact on the total costs. Material losses due to slicing wafers from ingots are one of the main reasons. Ribbon technologies can avoid these problems by producing wafers directly out of the silicon melt. We focus on the Ribbon on Sacrificial Template (RST) method which uses carbon-based substrates to cast silicon wafers. RST wafers have effective minority charge carrier diffusion lengths in the range of ~120 µm. Thus, the potential for good cell performances is given. A high efficiency solar cell process developed for defect-rich multicrystalline silicon materials at the University of Konstanz was applied on RST wafers. The goal was to gain insight into the material quality and properties to provide feedback for the wafer production. With over 14%, we can present the so far highest obtained solar cell efficiency for this material.
Keywords: RST, Ribbon Silicon, Cost reduction

1 INTRODUCTION

Today's costs of silicon wafer material for a photovoltaic module are around one third of its total production costs [1]. Therefore, there is a substantial interest in the development of a kerf-loss free and thus cost-efficient silicon wafer production. Also the wafer thickness is a relevant parameter for reducing material costs. One method amongst various technologies for direct wafer production [2] is the Ribbon on Sacrificial Template (RST) process [3]. In this casting process, molten silicon is directly crystallized on a carbon based substrate. Afterwards, the substrate is removed by a high-temperature burn-off step. This method is successfully applied by the company Solarforce (France), where wafer thicknesses from 50 µm up to 300 µm can be achieved. In this work p-type RST wafers with an average thickness of 130 µm and a base resistivity of 3 Ωcm were used. A minority charge carrier lifetime of 16 µs after phosphorous diffusion (gettering) and SiN_x firing (surface passivation and hydrogenation) has been observed. Former studies on p-type RST wafers showed cell efficiencies of up to 11.7% with evaporated contacts [4] and 11.5% with a screen-printing based cell process [6]. However, material quality is evolving and may not be directly comparable.

Determination of the solar cell efficiency potential and the characterization of RST material are of immanent relevance for future development and competitiveness of the RST technology. In this work, we apply a high efficiency solar cell process which was developed for defect-rich multicrystalline silicon materials such as e.g. RGS (Ribbon Growth on Substrate) or EFG (Edge-defined Film-fed Growth) at the University of Konstanz [5].

2 MATERIAL PROPERTIES

2.1 Casting process

The RST casting process is presented in figure 1. A carbon-based carrier is pulled through molten silicon, which directly crystallizes on the substrate surfaces. The substrate is removed by a high-temperature burn-off step afterwards.

The vertical pull direction results in a crystal growth of elongated grains with a varying size in the range of ~1 cm^2. Due to de-coupling of pulling and crystallization direction, a high wafer production speed in the order of 5 cm per minute is possible.

The thickness of the ribbon wafers can be varied from 50 µm up to 300 µm by changing casting parameters like pulling speed and temperature. For the cells presented in this work, the wafers had a thickness of 110-150 µm.

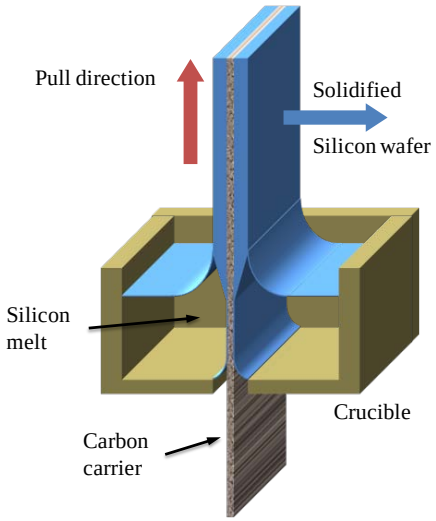

Figure 1: Schematics of the RST casting process [6]. A carbon-based carrier is pulled through molten silicon, which directly crystallizes on the substrate surfaces.

2.2 Material quality

The minority charge carrier lifetime is one of the most important material parameters for solar cells. To determine the average lifetime level for the processed RST wafers, some samples (originating from the same casting batch) were measured via QSSPC (Quasi Steady-State Photo Conductance) and PL (Photo-Luminescence imaging). Figure 2 shows a PL image of a RST wafer after a phosphorus gettering step. The emitter generated for gettering was chemically removed and the surface was passivated by a 30 nm thick Al_2O_3 layer after a RCA cleaning. The elongated grain structure is clearly observable. Regions of average lifetime values are intermingled by grains of increased charge carrier lifetimes of up to 30 µs. With a QSSPC measurement on a wafer after gettering and SiN_x:H firing an average

lifetime of up to 16 µs at an injection level of $1 \cdot 10^{15}$ cm^{-3} was observed.

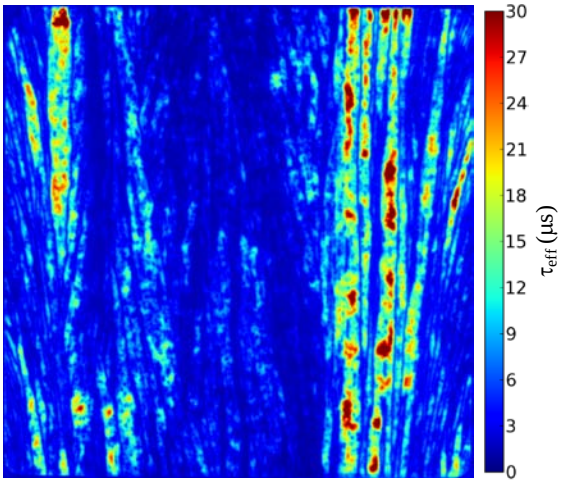

Figure 2: PL image of a 5x5 cm^2 RST wafer after a phosphorus gettering step. Lifetime is calibrated by a QSSPC measurement.

A more detailed analysis of RST wafer lifetimes was done on another batch of wafers but with a lower bulk resistivity of 0.5 to 1 Ωcm. Average lifetimes of about 11 µs with maximal values of over 13 µs were observed.

3 CELL PROCESS

A photolithography based solar cell process, developed for defect-rich multicrystalline silicon materials at the University of Konstanz (UKN) [5], was applied on the RST wafers. This was done to ensure that the cell results reflect the material potential by avoiding limitations of e.g. an industrial-type screen-printing based cell process. RST wafers have two different surfaces due to the unique crystallization method. The smooth side (melt) was in contact with the molten silicon during casting. The slightly rougher side (mold) was in contact with the carbon based substrate. To investigate the influence of the different surfaces, cells were produced both with the emitter on the smooth side and on the rougher side. The UKN standard photolithography based solar cell process uses a full area Al-BSF. However, material and cell process induced point shunts were observed on carbon-rich silicon ribbon materials e.g. by the commonly applied Al-BSF process [7]. To investigate and circumvent these possible problems, a solar cell process featuring a locally contacted rear side via Laser Fired Contacts (LFC) [8] was applied to some RST wafers. For monitoring the cell process, block-cast multicrystalline wafers (mc) with a bulk resistivity of 0.5–1.5 Ωcm were processed with the RST samples.

The UKN photolithography based cell process is shown in Figure 3. The original wafer size is 5x5 cm^2. Four 2x2 cm^2 cells are defined by the photolithography metallization on these source wafers. After metallization, the four small cells are cut out of the wafer by a dicing saw. More details about the cell process and efficiencies reached on several other materials can be found in [5], [8].

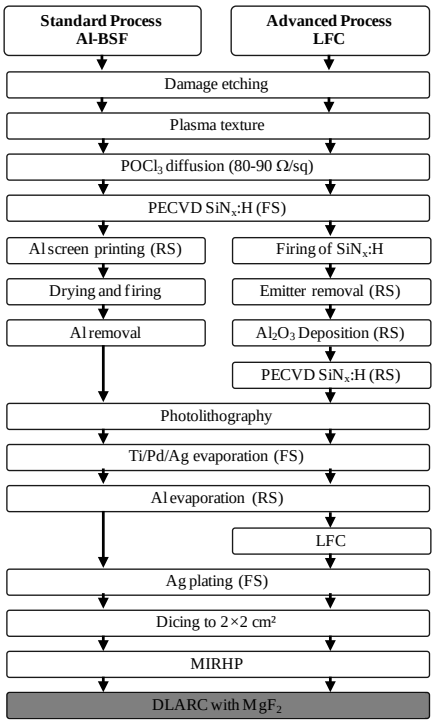

Figure 3: Flow chart of the applied solar cell processes with full Al-BSF and with dielectric rear side & LFCs. The double layer anti-reflection coating (DARC) is optional.

4 CELL RESULTS

4.1 Wafer side

The best cell results were obtained by choosing the smoother wafer side (surface that was in contact with the molten silicon in the casting process) for the emitter location. In table I the mean cell performances of RST solar cells with a single layer anti-reflection coating (SARC) are shown. The average is taken from the number of cells as indicated in table I. The results are split into cells with the emitter on the rougher side (mold), here called cell type A, and with the emitter on the smooth side (melt), here called cell type B.

Table I: Mean cell performances of RST cells. The label type A (mold) and type B (melt) indicates the location of the emitter.

Type/average Process	FF (%)	j_{sc} (mA/cm^2)	V_{oc} (mV)	η (%)
Type A/(10) Al-BSF	49.8	29.8	346	5.7
Type B/(3) Al-BSF	75.7	30.6	564	13.1
Type A/(10) dielectric RS	45.0	26.3	409	5.2
Type B/(12) dielectric RS	71.7	30.1	564	12.2

All cell parameters, especially fill factor FF and open circuit voltage V_{oc} suffered by locating the emitter on the rougher mold side. These results already define future handling of RST wafers.

A first explanation for the diverse results is the high shunting probability of the type A cells which is visible in figure 5. The range of values for open circuit voltage (cell type B) for Al-BSF cells and the LFC cells with dielectric rear side are comparable. In contrast, the mean short circuit current densities are higher on Al-BSF cells.

4.2 Best cells

Table II shows the best cell results of both cell processes. The results of the multicrystalline references are also shown.

Table II: Cell parameters of the best solar cells from RST and the mc references.

Material/ Process	FF (%)	j_{sc} (mA/cm²)	V_{oc} (mV)	η (%)
RST/ Al-BSF	77.9	30.4	569	13.5
RST/ dielectric RS	76.5	30.8	577	13.6
mc/ Al-BSF	79.1	34.2	621	16.8

For the best RST cell of the standard Al-BSF process, a thermally evaporated MgF_2 layer was deposited on top of the SiN_x. Due to this double layer anti-reflection coating (DARC) and the resulting gain in j_{sc}, the cell efficiency was increased to 14.1% ($\Delta\eta = 0.6\%_{abs}$). Table III shows the performance of this cell before and after applying a DARC.

Table III: Results of the best performing RST solar cell before and after application of a DARC.

Material/ coating	FF (%)	j_{sc} (mA/cm²)	V_{oc} (mV)	η (%)
RST SARC	75.1	31.1	575	13.5
RST DARC	75.5	32.4	576	14.1

5 DISCUSSION

Table II shows that for RST material similar maximal efficiencies can be reached with both applied cell processes. In figure 4 the Internal Quantum Efficiencies (IQEs) measured via spectral response (SR) of two RST cells are shown. The impact of the dielectric rear side in the average cell results is not as strong as would be expected by the higher IQE in the long wavelength regime. These limitations in cell parameters indicate variations in material quality. The effective minority charge carrier diffusion length extracted by a Basore-fit [9] to the IQE curves was in the range of 110-130 µm (for both processes).

Because of inhomogeneous etching of different crystal orientations, polycrystalline materials like RST cannot be textured by industrial standard alkaline etching solutions. Instead, a plasma texture was applied. The light trapping of plasma textures is not as efficient as e.g. by pyramid textured surfaces. But this deficit can partly be reduced by applying a DARC. With the resulting gain in j_{sc}, the best cell efficiency was increased to 14.1% with a total gain of $\Delta\eta = 0.6\%_{abs}$.

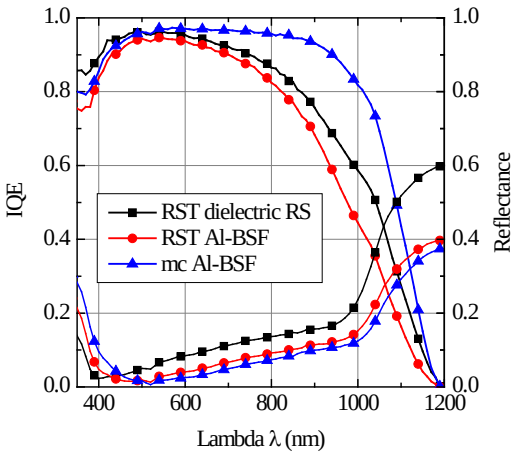

Figure 4: IQE and reflection of the best cells from RST wafers with dielectric rear side & LFCs (black, square) and Al-BSF (red, circle). A block-cast mc reference cell with Al-BSF is also shown (blue, triangle).

The thickness of the SiN_x ARC was not optimized for the DARC, so that a further increase in j_{sc} in an adjusted cell process is expected.

By comparing type A and type B cells in table I, it is obvious that the location of the emitter is of high importance for the cell performance. In figure 5, illuminated Lock-In Thermography (iLIT) shows enhanced recombination and shunting by locating the emitter on the substrate side. The second diode saturation current densities are in the range of 10^{-7} A/cm². It seems to be likely that carbon from the substrate heavily contaminated this wafer side. For future research depth-dependent SIMS measurements are advised.

The Electro-Luminescence image (EL) in figure 5 was carried out with an excitation current density of about 90 mA/cm². Cells of type A showed explicitly lower signals compared to cells of type B. Hence the measurement time for cells of type A was doubled for a better signal to noise ratio. This demonstrates the enhanced recombination which is to be expected from the cell results. Many recombination active grain boundaries and some inactive spots are visible. A comparison with the laser beam induced current image (LBIC) in figure 5 relates those areas to regions which generate low currents and hence low IQE regions. The LBIC scan was carried out with a spatial resolution of 50 µm and an excitation laser with a wavelength of 980 nm. This wavelength corresponds to a penetration depth of around 100 µm. This ensures that the whole wafer bulk is contributing to the signal. The open circuit voltage of RST cells of type B was in average V_{oc}=564 mV. The limitation of V_{oc} seems to be the result of low lifetimes (respectively high recombination), caused by a contamination originating from the substrate. Regarding type B cells in table I, it can be stated that the mean values of the IV cell parameters are comparable between the two different cell processes. A higher mean short circuit current density j_{sc} was observed on Al-BSF cells. This could be attributed to the optical and surface passivation properties of the two different cell processing approaches. The advanced cell process with LFCs was not optimal for RST wafer and has to be adapted in future experiments. Also, the Al-

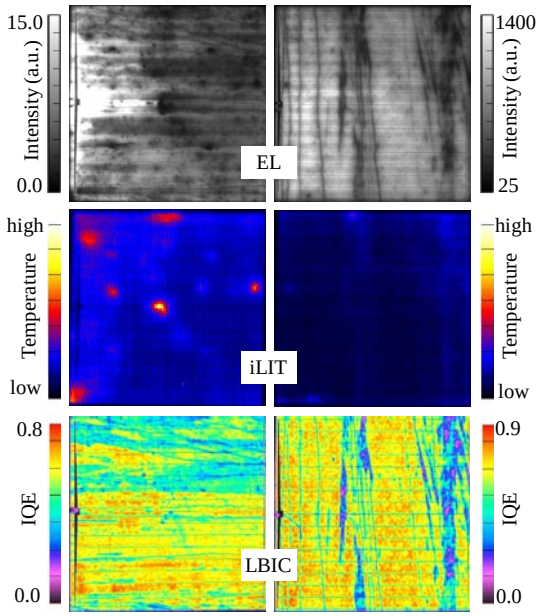

Figure 5: Comparison of EL, iLIT and LBIC on a cell of type A (left) and type B (right).

gettering step is missing for the LFC based process. The lowered fill factor for the advanced process seems to be a problem in context of material quality variations (when comparing it to the results of the best cells).

The illuminated IV measurement curve of the RST solar cells was fitted with a 2-diode-model. Hence the shunt resistance R_{Shunt} and series resistance R_s could be approximately gained. Cells with efficiencies below 10% were neglected because a fit with the 2-diode-model could not be satisfactorily applied in these cases. In Figure 6 the measured fill factor is plotted versus R_{Shunt}. A strong dependence of the FF from R_{Shunt} is clearly observable for R_{Shunt} <2000 Ωcm^2. For higher values of R_{Shunt} the FF saturates at about ~76.5%. The lowered fill factors compared to the mc reference (table II) cannot exclusively be explained by the shunt resistances.

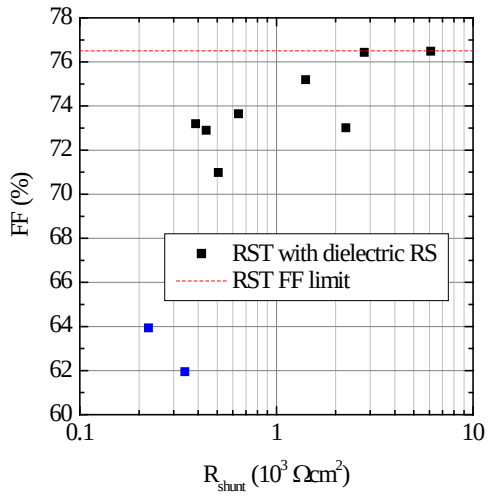

Figure 6: Fill factors of RST cells with dielectric rear side and LFCs is plotted against the shunt resistance R_{Shunt} (gained from fitting the 2-diode-model to the illuminated IV curve).

Also the series resistance which has average values of R_s = 0.4 Ωcm^2 is not accountable. But recombination active grain boundaries and impurities as shown in the EL image in figure 5 have an appreciable influence on the quality of the space charge region and hence on the saturation current density j_{02}. This is one of the main reasons for the limitation of the fill factor of RST solar cells. Also distinct point and areal shunts which can be seen in the iLIT image of figure 5 contribute to higher j_{02} and lower R_{Shunt} values. Experiments with fine grained multicrystalline silicon ribbon in the past [7] showed in general an empirical limitation in FF to ~78%.

5 CONCLUSION AND OUTLOOK

RST material has the potential to be a cost saving alternative to block-cast multicrystalline silicon. By applying a photolithography based solar cell process on RST wafers, the highest efficiency obtained so far could be demonstrated on 2x2 cm² lab-type solar cells. The efficiency of over 14% is very promising for these low cost silicon wafers. Since this photolithography based cell process was already successfully applied on other ribbon materials, the question of its applicability on RST wafers could also be answered. This enables the determination of solar cell efficiency potential of this material and is thus a tool for further wafer quality improvement.

Due to the unique casting process, RST wafers have two different surfaces. By locating the emitter on the smooth side the best cell results could be obtained. On the other hand, processing the emitter on the rougher side leads to worse cell results and a higher statistical spread of cell performances. The open circuit voltage of the processed samples is restricted to V_{oc} = 577 mV with an average of V_{oc} = 564 mV. This can mainly be attributed to the material quality and its variation. With j_{sc} >30 mA/cm^2, the average short circuit current density is at a good level. For the fill factors of the processed RST solar cells less room for improvement is expected. This is a consequence of increased saturation current densities j_{02} due to shunts and recombination. More detailed investigations by spatially resolved characterization techniques like EL and iLIT revealed those major loss mechanisms on RST cells. Higher efficiencies are expected on thinner RST wafers and adapted cell processes in the near future.

6 ACKNOWLEDGEMENTS

We want to gratefully thank Solarforce (France) for providing the RST wafer material. The financial support from the BMU project FKZ 0325079 is gratefully acknowledged in particular for the characterization equipment.

7 REFERENCES

[1] C. Del Cañizo, G. Del Coso, and W. Sinke, Progress in Photovoltaics, 17(3) (2009) 199.

[2] G. Hahn, S. Seren, M. Kaes, A. Schonecker, J.P. Kalejs, C. Dubé, A. Grenko, C. Belouet, Proceedings 4th WC PVEC, (2006) 972.

[3] C. Belouet, *Growth of silicon ribbons by the RAD process*, Journal of Crystal Growth, 82 (1987) 110.

[4] A. Focsa, A. Slaoui, S. Schmitt, F. de Moro, E. Jolivet, C. Belouet, E. van Kerschaver, J. Robbelein, Proceedings 24th EU PVSEC, (2009) 1887.

[5] J. Junge, J. Ebser, S. Graf, B. Terheiden, S. Seren, G. Hahn, M. Käs, Proceedings 25th EU PVSEC (2010) 1722.

[6] J. Robbelein, E. Van Kerschaver, C. Belouet, E. Jolivet, A. Focsa, A. Slaoui, N.E. Posthuma, B.T. Chan, M. Monville, C. Bigot, J. Poortmans, Proceedings 24th EU PVSEC, (2009) 1788.

[7] S. Seren, Low Cost Solar Cells from Fast Grown Silicon Ribbon Materials, PhD Thesis, 2009, University of Konstanz, Germany.

[8] J. Junge, C. Strümpel, S. Seren, G. Hahn, A. Metz, M. Käs, Proceedings 23rd EU PVSEC, (2008) 1561.

[9] P.A. Basore, Proceedings 23th IEEE PVSC, (1993) 147.