N-TYPE MULTICRYSTALLINE SILICON SOLAR CELLS: BBr_3-DIFFUSION AND PASSIVATION OF P^+-DIFFUSED SILICON SURFACES

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ABSTRACT: The shortage of the p-type silicon (Si) feedstock and the high minority carrier lifetimes in multicrystalline (mc) n-type Si reported by different authors ([1]-[3]) make n-type mc-Si solar cell fabrication more and more interesting. Given the high electronic quality of the material – that is confirmed in our studies again – the task remains to develop an adapted solar cell process. A key feature of the concept presented here is the BBr_3-diffused emitter on the front side and the surface passivation of this emitter. We show that BBr_3 emitter-diffusion is possible without degradation of the high initial carrier lifetimes in the n-type mc-Si material - on contrary the diffusion even improves the average lifetime to a large extend. SiO_2 provides an excellent surface passivation of the p^+-Si surface. Application of PECVD SiN_x resulted in a decrease of the (implied) V_{oc} measured on lifetime test-structures as well as on solar cell level. As an alternative, a low temperature surface passivation process by PECVD SiC_x is investigated. First trials resulted in a very promising value for the emitter saturation current J_{oe}: 180 fA/cm^2 for a 90 Ω/sq emitter. N-type Si solar cells with SiO_2-passivated BBr_3-emitter were processed in laboratory scale (area of 4 cm^2) with an efficiency of 15.2% on mc and 16.4% on Cz-Si. With an industrial screen printing process 14.1% and 14.8% were obtained on an area of 12.5 x 12.5 cm^2 on n-type mc-Si and Cz-Si respectively.

Keywords: Silicon, n-type, Multicrystalline

1 INTRODUCTION

The use of n-type mc-Si offers one possibility to attenuate the actual feedstock crisis. In addition, compared to p-type Si, n-type mc and Cz-Si have the following advantages:

- higher bulk diffusion length of the minority carriers
- lower sensitivity to metallic impurities [4], [5]
- no degradation of the Si bulk by boron-oxygen-pairs

Based on the high initial carrier lifetime in the mc-Si material, a suitable solar cell process should lead to cells with high conversion efficiencies. Work on the development of such a process is presented in this article. A prerequisite is that the process maintains or even improves the high carrier lifetime. In this concern, one important point is the emitter diffusion. We use BBr_3-diffusion in an open tube furnace, since it provides the required cleanliness and thus the bulk lifetime is maintained after emitter diffusion [3], [6]. Directly connected to the emitter diffusion is the passivation of the front surface. The surface passivation quality of SiO_2, PECVD SiN_x and PECVD SiC_x on p^+ -doped Si surfaces is investigated

2 MATERIAL PROPERTIES

The n-type mc Si wafers used for the investigations presented here, originate from two different Sb-doped directionally solidified ingots produced at Deutsche Solar. The minority charge carrier lifetimes measured on as-grown wafers from the middle of the ingots are 120 µs for ingot A and 166 µs (Figure 1) for ingot B – averaged over 12.5 x 12.5 cm^2 respectively. The specific resistivity of the wafers from these ingots is around 1 Ohm·cm. The n-type Cz-Si, used as a reference in solar cell processing and for emitter passivation experiments reveals a minority charge carrier lifetime of 450 µs and a resistivity of approximately 3 Ohm·cm.

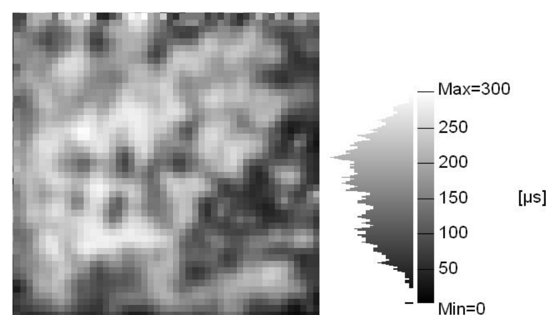

Figure 1: µW-PCD-mappings (microwave-detected PhotoConductance Decay) of the as grown carrier lifetime in Sb-doped n-type mc-Si. Average lifetime: τ_{eff} = 160 µs.

3 BBr_3-DIFFUSION

3.1 Diffusion profiles

For the small area laboratory cells, the boron emitter diffusion has been carried out at 900°C leading to a sheet resistance of 70 Ohm/sq directly after diffusion. After the diffusion, the boron glass was removed by HF-etching, but the wafer surface still remains hydrophilic. This is due to the so called Boron Rich Layer (BRL – a highly conductive layer with a high boron concentration, containing BSi_x [7]), which is formed during the BBr_3-diffusion. A subsequent thermal oxidation is performed to convert the BRL into boron glass, followed by a deglaze with HF. Figure 2 shows the change of the emitter profile (measured with the Electrochemical

Capacitance-Voltage (ECV) method) after the different process steps and the corresponding sheet resistances. Each thermal oxidation leads to a depletion of boron at the surface, since its solubility is higher in SiO_2 than in Si. In order to avoid this depletion – which could reduce the resulting V_{oc} and its long-term stability [8] – the diffusion process has been modified: instead of two furnace steps (diffusion – deglaze – oxidation of BRL), the BBr_3-diffusion was followed immediately by a thermal oxidation in the same furnace step ("in-situ" oxidation). In this configuration, the oxygen diffuses through the boron glass and oxidizes the BRL. With this process sequence, a hydrophobic wafer surface (i.e. BRL completely removed) has been obtained with one furnace step. The corresponding ECV profile in Figure 2 exhibits virtually no surface depletion. This is explained by the fact, that here the boron glass, which acts as diffusion source, is still present during the oxidation step. Consequently, the out-diffusion of boron into the SiO_2 is counterbalanced by the supply of boron from the boron glass. This improved diffusion process has been used for the fabrication of industrial screen-printed cells (see section 5).

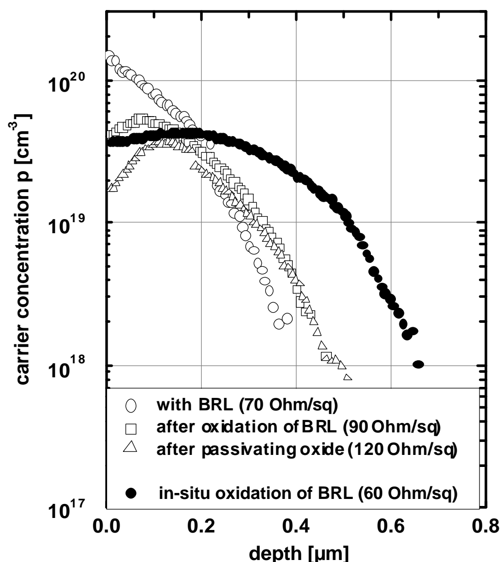

Figure 2: Diffusion profiles from two-step diffusion process compared to one-step "in-situ" process measured by ECV method.

3.2 Impact of BBr_3-diffusion on carrier lifetime

The two-step BBr_3 emitter diffusion has been shown to maintain the high bulk lifetime of the mc-Si. In Figure 3, the effect of the complete "industrial" solar cell process (see section 5) on the bulk lifetime of Sb-doped material (ingot A) is shown. The lifetime measurements have been performed with microwave-detected PhotoConductance Decay (µW-PCD) and a chemical passivation (iodine/ethanol solution) of the surfaces. The emitter and the Back-Surface Field (BSF) have been removed from the processed wafer with a mixture of HF, HNO_3 and CH_3COOH (CP6). The result was a largely improved lifetime after solar cell processing.

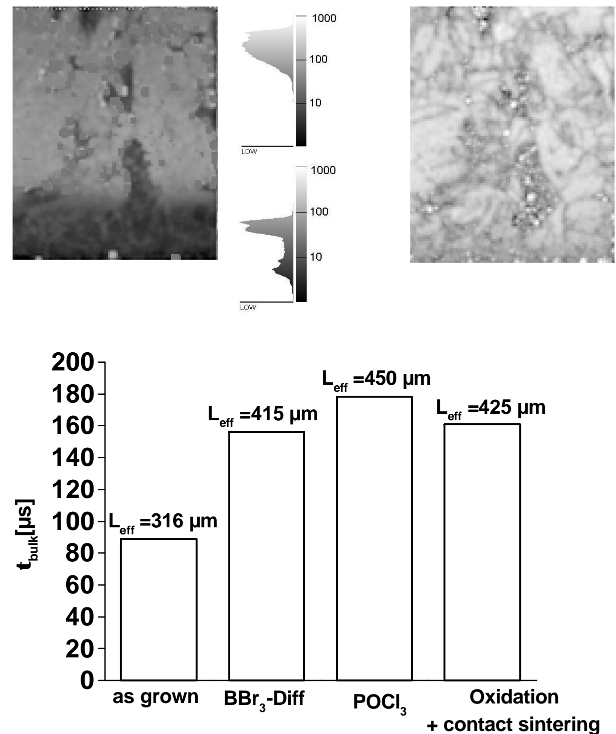

Figure 3: top: µW-PCD mappings of the bulk lifetime of a 10 x 12.5 cm^2 n-type mc Si wafer (from the edge of ingot A) a) before and b) after process for large screen- printed cells (section 5). Bottom: evolution of the lifetime (averaged on 5 x 5 cm^2) during cell process.

4 EMITTER PASSIVATION

Applying a thin (10 nm) thermally grown SiO_2, an emitter saturation current (J_{oe}) of 80 fA/cm^2 has been obtained on p^+np^+ test structures (90 Ohm/sq BBr_3 on both sides of an n-type 3 Ohm·cm cm Cz-Si wafer) measured with Quasi Steady-State PhotoConductance (QSSPC). Prior to SiO_2 passivation, the J_{oe} measured on the same samples was around 1000 fA/cm^2. These values are in good agreement with e.g. [9].

As a low temperature approach which in addition requires no extensive wet chemical cleaning – particularly important for the screen-printed industrial cells – the passivating properties of PECVD SiN_x have been tested on the p^+np^+ samples. The QSSPC measurements (Figure 4) showed an injection level dependent J_{oe} (as already reported by [10]) which makes the determination of J_{oe} ambiguous. To be able to compare the different means of surface passivation, we follow the example of [10] and use the implied V_{oc} as a criterion. It has been determined to 575 mV for SiN_x coated samples, compared to 596 mV for the bare, unpassivated emitter. This result is confirmed by 4 finished n-type Cz-Si cells, with an average V_{oc} of 593 mV without any front surface passivation which dropped to 581 mV after deposition of SiN_x. A possible explanation is an increased Surface Recombination Velocity (SRV) by the field effect of the fixed positive charges Q_f in the SiN_x layer. On moderately doped p-substrates (doping below $1x10^{15}$ cm^{-3}), this Q_f is high enough to accumulate electrons at the surface in order to create a n-conducting surface layer ("inversion") and

thus a p-n junction. This p-n junction provides a surface passivation in the same way as a floating emitter. On the heavily p-doped surface of the boron emitter however, this increase of the electron concentration n_e at the surface approaches the concentration of the holes n_p which leads to an increase of the SRV (SRV would be maximum for n_e=n_p). Another hypothesis to be tested is e.g. the possibility of partial inactivation of the boron in a thin surface layer by hydrogenation from the SiN_x.

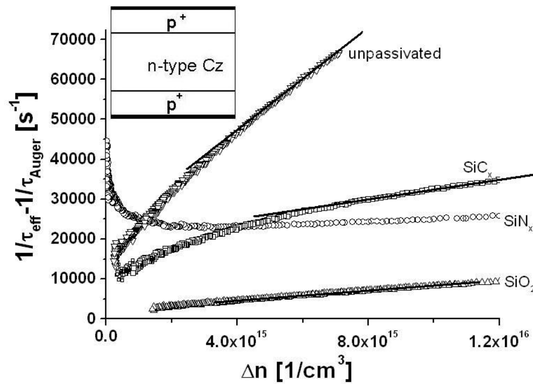

Figure 4: QSSPC-measurements - J_{oe} from slope method. Investigated coatings: SiO_2, SiN_x, SiC_x

The search for an alternative passivation scheme with the same advantages as PECVD SiN_x lead to PECVD SiC_x, which has been reported to provide excellent surface passivation on p-type Si substrates [11] with Q_f being in the same order of magnitude as for SiO_2 [12]. An adapted SiC_x coating was applied to the p^+np^+-samples. QSSPC measurements showed a weak injection level dependency of J_{oe} permitting an estimation of J_{oe} to 180 fA/cm^2 for a Si-rich SiC_x layer (high absorption in the UV-range) and 300 fA/cm^2 for a stack of only a thin layer (10-12 nm) of Si-rich SiC_x and a thicker layer of C-rich SiC_x (to obtain a good antireflection coating with low absorption). For this stack, the implied V_{oc} has been determined to 612 mV (Figure 5). It is planned to further optimize the SiC_x-coating towards better surface passivation to reach even lower J_{oe} and thus higher V_{oc}.

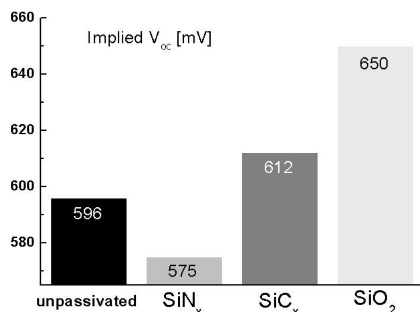

Figure 5: Comparison of the implied V_{oc} obtained by the different surface passivations (determined with QSSPC-measurements on p^+np^+ samples)

5 SOLAR PROCESSING AND RESULTS

5.1 Passivated front emitter and full rear contact

The solar cell process applied to the n-type mc Si material presented in section 2 is shown in Figure 6. With an oxide-passivated 90 ? /sq BBr_3-emitter and a fully metallized rear side, efficiencies of 11% have been reached, which resulted in 14.7% efficiency after a non-optimized antireflection coating [6].

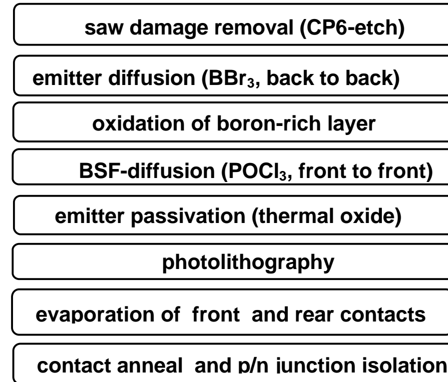

Figure 6: Solar cell process scheme, front and rear contacts are formed by a Ti/Pd/Ag-stack

5.2 Cells with local rear contact

In order to improve the effective surface recombination velocity on the rear side, the process shown in Figure 6 has been slightly modified: photoresist has been deposited also on the rear side of the cell for opening the rear side SiO_2 locally. In this way a simplified PERT-structure (homogenous diffusions on both sides – no selective emitter, no heavy diffusion on the point contacts) has been obtained. In one experiment, a considerable improvement in the long wavelengths response of Cz-cells could be observed (Figure 7 top). For reasons which are up to now unexplained, the short wavelength response of these cells did not reach the excellent quality reached in a previous experiment. This applies also for the mc cells which, in addition, only show a slight improvement of the rear side (Figure 7 bottom).

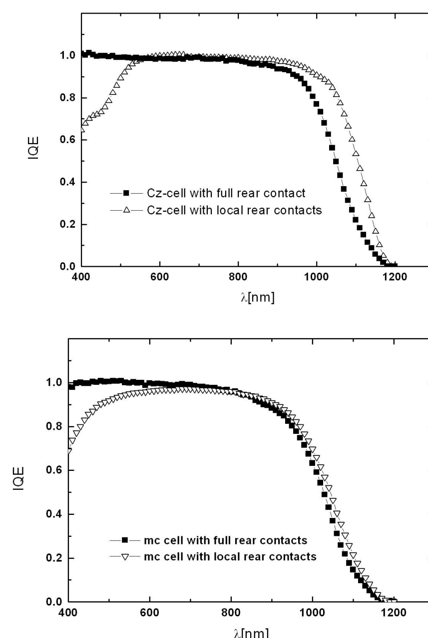

Figure 7: IQE of SiO_2-passivated Cz-Si (top) and mc-Si (bottom) cells with full and open rear contacts

Despite the lack of front surface passivation and a rather low fill factor (due to metallization problems) the best mc-Si solar cell with an optimum double-layer antireflection coating (DLARC) reached a respectable efficiency of 15.2% (Table I).

FF [%]	J_{sc} [mA/cm^2]	V_{oc}[mV]	? [%]
74.3	34.0	601	15.2

Table I: Best solar cell on n-type mc-Si from process including local rear contacts, with DLARC

5.3 Large area screen-printed cells

The fabrication of screen printed solar cells on 12.5 x 12.5 cm^2 mc n-type wafers has been performed using an adapted process. Since in the back-to-back (and front-to-front) configuration some diffusion on the edges of the covered side could not yet be avoided, it has been replaced by coating one wafer side respectively with PECVD SiN_x as a capping layer. In addition a stronger BBr_3-diffusion (60 Ohm/sq, with in-situ oxidation of the BRL) has been applied. The emitter surface has been coated with a SiO_2/SiN_2-stack, which lead to a good surface passivation (the 20nm thick SiO_2 apparently shields the emitter from the negative effect of the SiN_x) and serves as ARC. This process resulted in solar cell efficiencies above 13.5 %, the I/V parameters of the best cells are shown in Table II.

	FF [%]	J_{sc} [mA/cm^2]	V_{oc} [mV]	? [%]
mc-Si	74.5	31.5	599	14.1
Cz-Si	72.8	33.3	610	14.8

Table II: Best industrial solar cells – the low fill factor is due to a high series resistance; a FF of 78 % would lead to 15.8 % efficiency on Cz-Si.

6 CONCLUSIONS AND OUTLOOK

n-type mc-Si has been shown to have high initial minority carrier lifetimes which are considerably improved within the solar cell process, which includes BBr_3 emitter diffusion, $POCl_3$ BSF diffusion and the growth of a 10 nm thermal SiO_2-layer for surface passivation. Best surface passivation of the 90 Ohm/sq BBr_3 emitter has been obtained by a SiO_2 layer (J_{oe} = 80 fA/cm^2). Measurements of PECVD SiN_x (direct plasma with low frequency as well as remote plasma with microwave frequency), lead to an injection level dependent J_{oe} which made it impossible to extract an unambiguous value for J_{oe}. Thus, the implied open circuit voltage has been used to compare the different surface passivations. This is possible since all the test structures were fabricated on the same n-type Cz material - i.e. with the same bulk lifetime, which was tested to remain unchanged after the respective process steps. The result was a decrease in V_{oc} compared to the unpassivated samples (575 mV vs. 596 mV). The SiN_x used in this work was optimized for the passivation of a standard P-doped n^+-emitter of p-type cells. As the density of the fixed positive charges in PECVD SiN_x ranges between 1 x 10^{11} cm^{-2} (like SiO_2 and PECVD SiC_x [12]) and 5 x 10^{12} cm^{-2} [13] it still has to be clarified if SiN_x with a lower charge density may provide a surface passivation on p^+-Si.

PECVD SiC_x has been successfully tested to be an alternative low-temperature process for surface passivation of p^+-Si surfaces. First experiments lead to a J_{oe} of 190 fA/cm^2 for a thick Si-rich SiC_x layer and to 300 fA/cm^2 for a stack consisting of a thin Si-rich layer and a layer of C-rich SiC_x. The stack features better optical properties. Further optimization of the PECVD SiC_x-coating is in progress, with the aim to apply it on screen-printed cells.

The efficiency of the best screen printed cell on a 12.5 x 12.5 cm^2 n-type mc Si wafer was 14.1% using a SiO_2/SiN_x-stack on the front surface. On a laboratory scale (A = 4 cm^2, photolitographically defined contacts), an efficiency of 15.2% has been reached for mc-Si and 16.4% a Cz-Si [6]. Concerning the laboratory cells, the reproducibility of the passivation of boron diffused mc and Cz-Si by SiO_2 has to be improved and the rear surface recombination velocity needs to be further decreased. For the latter, n-type mc cells in PERC-design are currently under investigation. Combining the high minority carrier diffusion length measured in the processed material with the passivation quality already obtained with SiO_2, there is a potential for high efficiencies on n-type mc-Si.

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References

[1] A.Cuevas et al., *N-type multicrystalline Silicon: a stable high lifetime material*, proc. of the 3rd WCPEC, Osaka, May 2003
[2] R. Kopecek et al., *N-type multicrystalline Silicon: material for solar cell processes with high efficiency potential* proc. of the 31st IEEE PVSC, Orlando 2005
[3] J. Libal et al., *Properties of N-type multicrystalline Silicon: lifetime, gettering and H-passivation*, proc. of the 19th EPSC Paris, 2004
[4] L.J. Geerligs and D. Macdonald, *Base doping and recombination activity of impurities in crystalline silicon solar cells*, Progress in Photovoltaics 12, 309 (2004);
[5] Martinuzzi et al, *n-type Si and plasma immersion doping for solar cells*, proccedings of the 14th NREL-wokshop, 2004
[6] J.Libal et al., *N-type multicrystalline silicon solar cells with BBr_3 diffused front junction,* proc. of the 31st IEEE PVSC, Orlando, 2005
[7] M.S. Bae, PhD thesis, Columbia University, New York 1979
[8] Zhao et al., *Performance instability in n-type PERT silicon solar cells*, proc. of the 3rd WCPEC, Osaka 2003
[9] A Cuevas et al, *The Recombination Velocity of Boron Diffused Silicon Surfaces*, proc. of the 14th EPVSEC Barcelona, 1997
[10] M. Kerr, PhD thesis, Australian Nation University, Canberra, 2002
[11] I. Martín et al., *Surface passivation of p-type crystalline Si by plasma enhanced chemical vapour deposited amorphous SiC_x:H films*, Appl.Phys. Lett., 79 (14), pp. 2199-2201 (2001)
[12] I. Martín , PhD thesis, Universitat Politecnica de Catalunya, Barcelona, 2003
[13] A. Aberle, *Crystalline Silicon Solar Cells – Advanced Surface Passivation and Analysis*, Sydney 1999