

LARGE AREA SILICON LPE ON HIGHLY DOPED SILICON SUBSTRATES AND RESULTS OF RELATED THIN FILM SOLAR CELLS

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ABSTRACT: Large Area Silicon Liquid Phase Epitaxy (LPE) on different, most highly doped, silicon substrates is carried out. The main idea behind doing this is: to purify the top layer, about 10% of the bulk, to a reasonably doped starting material for the solar cell generation. A first result obtained was an efficiency of $\eta = 8.8\%$ on a related thin film solar cell ($A = 25\text{ cm}^2$), based on a LPE treated 0.02 Ohm cm CZ wafer. The purpose of the work is to examine if large area thin film LPE solar cells realized on cast multicrystalline silicon substrates from low cost metallurgical silicon feedstock can be one interesting track for the near solar cell future.

Keywords: Si Feedstock, LPE, Texturisation

1 INTRODUCTION

The limited availability of abundant low cost silicon for photovoltaic use is the main barrier for the development of solar cell industry in near future. About 50% of the cost of crystalline Si-modules are related to the substrate. The substrate costs almost equally comes from silicon feedstock, crystallisation, and wafering costs. The use of low cost upgraded metallurgical silicon instead of the high cost electronic grade silicon (EG-Si) could drastically reduce the cost of silicon. The upgraded metallurgical silicon will be referred as photovoltaic graded silicon (PVG-Si).

In conventional silicon solar cell, the substrate is active absorber, whereas, in this thin film silicon solar cell concept, the absorber is a thin silicon layer epitaxially grown on the substrate. In thin film silicon solar cell, the low cost of substrate may offset the extra cost of the epitaxial growth of thin absorber layer. However, the advantages of thin film Si solar cell technology rely on the availability of PVG-Si which requires lower energy consumption and low capital investment for a production plant.

2 PHOTOVOLTAIC GRADE (PVG) SILICON PRODUCTION

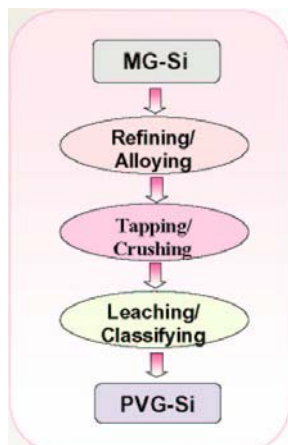


Figure 1: Process steps in the production of PVG-Si feedstock.

PVG-Si feedstock production at Elkem includes melting and alloying of metallurgical silicon to get a leachable alloy, casting and solidifying of this alloy and crushing it into 30 mm lumpy material, leaching with a suitable leach liquor to separate the pure Si crystals and classifying of pure Si crystals. The product is PVG-Si with main fraction in the range of 0.2-2.0 mm.

Fig. 1 shows schematic process steps for the manufacture of the PVG-Si feedstock.

3 SUBSTRATE CRYSTAL GROWTH AND WAFERING

The particle grain size for the raw PVG-Si powder of 0.2-2.0 mm, is a necessary consequence of the leaching process. Ingots from this feedstock are grown by directional solidification at Sintef in a Crystalox DS250 furnace. The ingot growth is controlled by temperature, crucible translation and the variable heat leak (VHL) system, which allows changes in heat flow through bottom of crucible. The directional solidification technique is shown to be an effective way to remove impurities except in the region near the top surface. The material is highly doped with boron and this element is not removed, leaving a material with a low resistivity ($\rho=15-40\text{ m}\Omega\text{cm}$). From the ingot either one or two $10 \times 10\text{ cm}^2$ blocks are squared out with further cutting off the bottom and top parts. Wafering is performed at an industrial location with a wire saw equipment to wafer thickness in the range of 300-350 μm . Average dopant density of the wafers are about $2\cdot 5\cdot 10^{18}\text{ cm}^{-3}$.

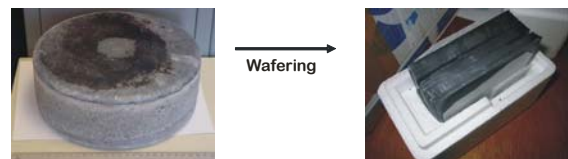


Figure 2: DS growth ingot followed by cutting in $10 \times 10\text{ cm}^2$ wafers.

4 LPE GROWTH PROCESS

In order to transform former small area laboratory LPE layer results[1, 2] from a previous EC funded project to a new LPE pilot reactor, an existing LPE apparatus was completely reconstructed at the University of Konstanz and enlarged, enabling to deposit about ¼ m² active layers at once, using batches of 14- 28 substrates of 10x10 cm². Layers of 10-30 µm thickness were grown from indium solution on the PVG-Si (and at an intermediate stage e.g. on highly doped CZ “equivalent”) wafers in the temperature range T≈1000°C-800°C. The melt-back of silicon substrate was used to saturate the solution without the need of electronic grade silicon sources, which is a scientific innovation in the field of large area silicon LPE solar cells. This layer growth process leads in the ideal case to a high quality LPE layer because of the different solubilities of impurities in indium and regrowing silicon. Although the substrates are doped by p=2·5·10¹⁸ cm⁻³, LPE layer doping concentrations profiles of p=2·10¹⁶-10¹⁸ cm⁻³ were achieved. The carrier concentration within the LPE layer varies from back to front, due to the temperature dependent solubility of p-type dopants, leading to an effective drift field for minority carriers and thus an increased effective diffusion length respectively.

The process shown in Fig. 3 (from left to right) was applied for epitaxial layer growth:

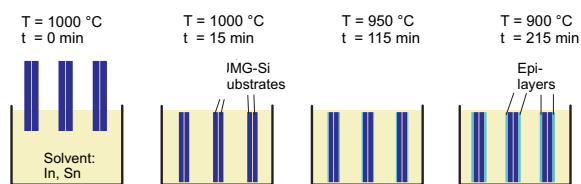


Figure 3: Principle of the Si-LPE growth for LPE layers on wafers from upgraded metallurgical silicon: Wafers are loaded back to back for one side growth. If bifacial LPE solar cells are considered, both sides could be coated.

In principle the indium solvent is saturated with Si at around 900°C and afterwards heated up to about 1000°C. Then wafers are placed into the melt, such that the melt is saturated again from Si of the substrate resulting in thinning of the wafer of about 15-30µm for each side. By cooling down the melt the LPE layer is grown. The highly doped substrate enables easy formation of the back contact, whereas the LPE layer acts as an active solar cell absorber. Residual impurities are expected to remain in the solvent because of the different solubility in epitaxial growing Si and in the melt.

The growth process was varied in some ways to overcome the problem of initially arisen pinholes (shunt in later solar cell) in the large area LPE layers. E.g. a more careful melt back showed a positive effect on homogeneity of the achieved layers and tiny growth steps alternated by tiny melt back steps resulted in the best LPE layers on large area so far.

To be able to grow an industry relevant throughput of LPE layers on 10 x 10 cm² wafers by the new LPE reactor, a lot of development work was needed. The

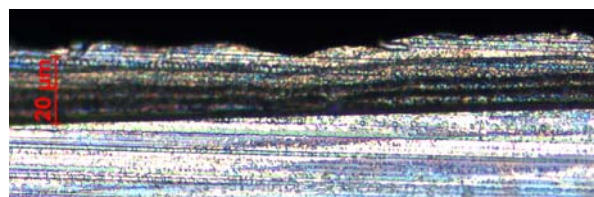


Figure 4: Cross-section of LPE layer grown in summer 2004, the four melt back/growth cycles can be observed in the ~20 µm layer.

most important task, how to place the wafers in the already determined dimensions of the crucible (which contains the melt) have to be answered by carrier design (Fig.5):

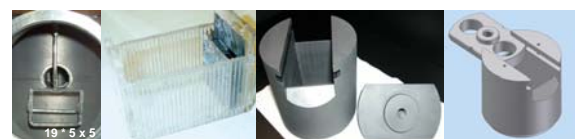


Figure 5: Carrier development 2002-2004: 5 x 5 cm² → 10 x 10 cm², quartz → graphite → pyrolytical graphite

First a hand made carrier from quartz glass was build for 19 5 x 5 cm² wafers. Soon a catalog of requirements for an ideal carrier was formulated. An important question is to find an adequate material. Graphite works better than quartz which leads to oxidation of the indium melt surface. A graphite carrier system, partly surface treated by pyrolysis is now in use. The new system is improved in detail, e.g. 2 clamp holes are included considering the temperature depending density of the melt.

After a time of stagnancy in LPE layer quality the process technology was audited. It resulted in the cleanest experimental conditions we have so far. By using special treated graphite and no more quartz, better hydrogen quality etc. nearly all problems are solved. But there is still a problem left: while thermalizing the wafers some cm above the melt, indium evaporates onto the wafer surface. It is assumed, that the indium inhibits the reduction of the residual natural oxide, which is always present on the wafer surface even after cleaning. The oxide layer compromises the melt-back step and promotes the formation of pinholes during subsequent epi-layer growth.

Therefore the next aim is to hinder the evaporating In to get in contact with the wafers. First it is realized in a very simple way, by adding a horizontal wafer between a shortly mounted stirrer and the vertical probes (Fig.6). The first results using this procedure looks promising. A reconstructed wafer carrier, which solves the mentioned problem by inclined wafer slots is in machining.



Figure 6: stirrer/ horizontal wafer in carrier/ latest carrier

5 ELECTROCHEMICAL MACROPOROUS TEXTURIZATION OF LPE LAYER

The electrochemical (EC) texturization [3, 4], and the associated low reflectivity and light trapping, is an important factor for the realization of efficient solar cells based on a thin LPE layer (30 μm) grown on a Si substrate. EC texturization treatments have been performed on bulk mc-Si and (100) CZ c-Si and on LPE layers grown over these two types of substrate.

With bulk materials of known resistivity, the efficacy of the EC treatment can be evaluated independently of the problems related to the epitaxial growth. We focused our studies on bulk Si with a resistivity similar to that of LPE layers grown on highly doped substrates ($5 \cdot 10^{16} \text{ cm}^{-3}$, 0.3 ohm.cm). Fig. 7 plots R_E of large samples (i.e. including several grains in the case of mc-Si) as a function of the resistivity.

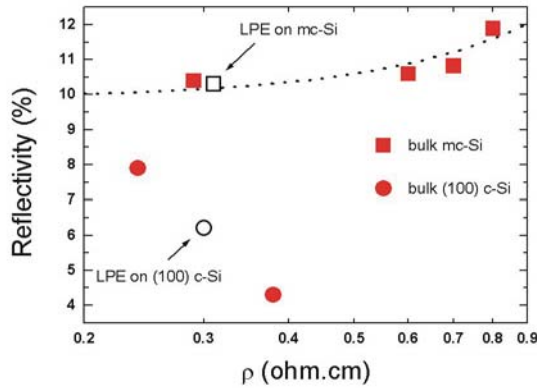


Figure 7: Measured R_E after EC texturization of multicrystalline (■) and monocrystalline (●) Si wafers as a function of the bulk resistivity. Expected R_E values (□, ○) for 0.3 $\Omega \text{ cm}$ LPE layer grown on crystalline substrates. R_E is calculated with AM1.5 solar spectrum over the 400 -1000 nm range.

We found that at 0.3 ohm.cm (LPE layer resistivity) the effective reflectivity (R_E) is $\sim 10.5 \%$ for mc-Si and should be $\sim 6 \%$ for c-Si (interpolate from the two data available). It is noteworthy that these values are considerably smaller than that measured on the same substrate after NaOH texturization (standard industrial treatment, $R_E \sim 20 \%$ and $\sim 12 \%$ on mc-Si and (100) c-Si).

Comparable R_E have been obtained after EC texturization of LPE layers. When grown on EG mc-Si substrate they were contained between 10.3 % and 16.8 %, with a mean value of 12.8 %. When grown on (100) CZ c-Si, R_E was between 6.2 % and 14.4 %, with a mean value of 10.4 %. In all cases, the texturization etches only 3 μm or less from the LPE layer, a limited reduction in thickness ($\sim 10 \%$).

We found that the relatively large spreading in R_E is a consequence of the presence of pinholes in the LPE layer. During the EC treatment, the anodic current flows from the substrate through the LPE and dissolve Si atoms at the surface in contact with the electrolyte (texturization). However, if there are areas of direct contact between the substrate and the electrolyte, the current avoids the more resistive LPE layer and the anodic dissolution (of the substrate) occurs mainly in these regions. After texturization, some LPE layers

exhibit R_E identical to that of texturized bulk materials (with the same resistivity). This indicates that these LPE layers were (almost) pinholes free.

6 SOLAR CELL GENERATION

Eleven runs were performed on LPE layers (with and without EC texturization) by means of common industry standards (POCl_3 -diffusion, SiN-ARC, screen-printing and firing-trough). Unfortunately, most cells were shunted due to pinholes in the LPE layers or improper surface conductivity. Efficiencies up to $\eta = 3\%$ were reached on multi-crystalline LPE layers grown on highly boron doped electronic grade silicon. Reference solar cells made from Elkem's solar grade silicon (0.2-0.3 $\Omega \text{ cm}$ resistivity, which is the preferred final resistivity of the LPE layers) without texturization reached efficiencies up to $\eta = 12.3 \%$.

FF [%]	j_{sc} [mA cm^{-2}]	V_{oc} [mV]	η [%]	p [cm^{-3}]	Remarks
49,7	23,8	600	7,1	$8 \cdot 10^{16}$	LPE on CZ-Si wafer 0.02 Ωcm , 4 cycles
57,5	25,1	605	8,8	$8 \cdot 10^{16}$	LPE on CZ-Si wafer 0.02 Ωcm , 5 cycles
73,8	27,4	616	12,3	$8 \cdot 10^{16}$	SoG-Si mc Reference
73,4	27,6	611	12,4	$8 \cdot 10^{16}$	SoG-Si mc Texturized Ref

Table I: Best 25cm^2 solar cell efficiencies reached so far on LPE layers grown on highly doped CZ substrates and on Elkem's SoG-Si wafers of 0.2 $\Omega \text{ cm}$ resistivity without LPE layer.

On reference wafers texturized by CNRS, efficiencies slightly higher than on untreated samples were possible. Previous results on texturized wafers showed minor performance. To phase out difficulties of LPE layer growth at grain boundaries and to overcome a temporary shortage of suitable wafer material, monocrystalline CZ-wafers (Electronic Grade, with high boron doping, 0.02 Ωcm) were used for LPE layer growth.

Solar cells processed on those LPE layers showed good V_{oc} , which indicates no shunting through pinholes or other discontinuities. Still there is a sub-optimal fillfactor (FF), which limits the overall performance on those LPE layers.

These limitations in FF on LPE layers can be caused by series and/or parallel resistances and/or recombination mechanisms.

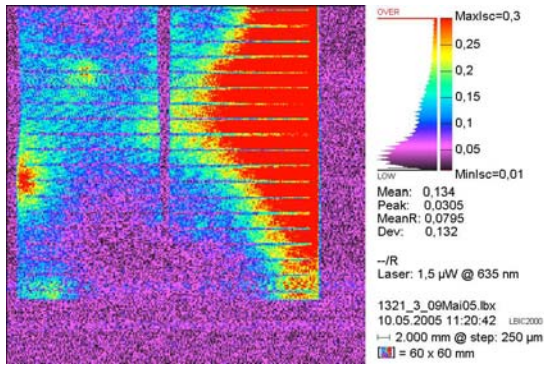


Figure 8: LBIC-Measurement of screen-printed solar cell processed on LPE layer on CZ wafer. Apparently, there is unwanted inhomogeneity.

Further investigations concerning adhesion problems of contact finger screen printed on EC texturized LPE layers were examined. For this purpose, alternative contacting technologies like evaporaton of Ti/Pd/Ag were being taken into account. To address the inhomogeneities on the LPE layers as well, we developed a photolithographic mask, which gave us the possibility to process nine 1cm² on 25cm² wafers.

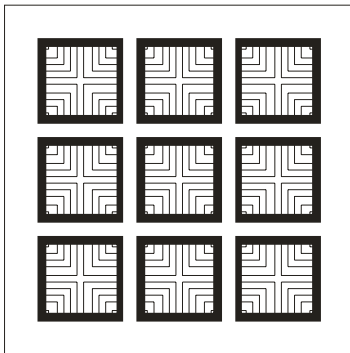


Figure 9: Design of photolithographic mask.

Solar cells processed with this mask received phosphorous diffusion and SiN-ARC by PECVD (industry standard). Then there was a photolithographic masking step to open SiN-ARC by plasma etching and HF dip. Finally, front contacts were processed by evaporation of Ti/Pd/Ag. Back contacts consist of evaporated Al. Some cells showed good V_{oc} higher than 500 mV, but removal of SiN-ARC by plasma etching was difficult, resulting in low fill factors.

Further examination of the texturisation on reference wafers led to solar cells with evaporated contacts but without SiN-ARC. Tempering and hydrogen passivation was achieved by MIRHP. These solar cells showed good fill factors (75%) and V_{oc} (590mV), but low I_{sc} (20mA/cm²) resulting in low efficiencies of η ~ 9%. Interpretation of these results is poor contact formation in the evaporation step on texturized wafers.

In Fig. 10 the promising development in efficiencies of 25 cm² LPE solar cells processed on highly doped substrate (0,02 Ωcm) since the beginnig of the project is shown.

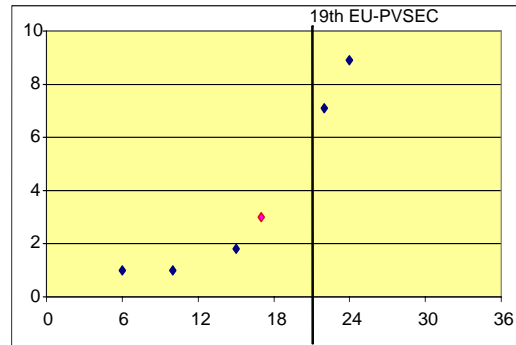


Figure 10: Efficiency (y axis) plotted vs. project month (x axis), exception: red dot indicates efficiency reached on LPE layer grown on Elkem 0,3 Ω cm solar grade silicon.

7 CONCLUSION

The availability of abundant low cost Si for PV power production at large scale is the main barrier for the future development of PV market. The low cost and abundant upgraded metallurgical PVG-Si appears to be a suitable feedstock for the production of wafer substrate for thin film silicon solar cells and modules. It is expected that solar cell of target performances could be achieved with the overcoming of the pinhole problem.

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