# PROGRESS IN MONOLITHIC INTEGRATED MONOCRYSTALLINE SI SOLAR CELLS

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ABSTRACT: The fast growing market of portable electronics demands solutions in solar power supply with high energy conversion efficiencies and a long time stability, which is so far not guaranteed by the monolithic series interconnection of thin film solar cells. In contrast monolithic integrated solar cells [1] based on monocrystalline silicon enable the series interconnection [2] of several unitcells on one wafer already during the applied screen-printing metallization and offer both high efficiency and long time stability. The output voltage of the so called HighVo solar cells is easily scaleable and therefore adjustable to different requirements. At University of Konstanz two different concepts of HighVo solar cells were developed, the Metallization Wrap Through (MWT) and the Emitter Wrap Through (EWT), whereas only the MWT types were considered in this study. We investigated possibilities to increase $J_{sc}$ and with it the efficiency of the cells. One option is alkaline texturing of the front surface for reduced reflection losses. In addition emitters with higher sheet resistance were studied due to their better blue response. The experimental results on MWT devices give reason to reach efficiencies greater than $\eta$=13% with optimized processing and $J_{sc}$ matched emitters in the near future.
Keywords: monolithic - 1: high voltage - 2: texturization - 3

## 1. INTRODUCTION

The increasing number of power intensive mobile consumer and telecommunication electronics opens an interesting field of research for new types of solar cells and mini modules. The requirements for these applications are well known and so far not really fulfilled by any of the existing concepts.

Output voltages of several volts, combined with rather high efficiencies well above present amorphous silicon thin film solar cell arrays, and of course a highly aesthetic appearance should be covered by an adequate solution.

Our approach is based on low cost crystalline Si production techniques combined with a monolithic integration of series interconnection. This idea assimilates the best of both worlds, which means that the advantage of monolithically integrated thin film modules [3] – no unit cells have to be interconnected after processing because of the unity of the device – is paired with the capacity of high efficiencies of crystalline silicon.

First experiments and investigations at University of Konstanz concerning the idea of monolithic integrated monocrystalline Si solar cells started three years ago [4-6] and led to several different so called HighVo solar cell concepts and geometries. In the present investigation only test structures of MWT HighVo solar cells were fabricated to simplify processing and result finding. The HighVo cells for future possible applications are supposed to be EWT HighVo solar cells with modified cell geometry, the so called “frame” geometry [4].

## 2. CONCEPT OF (MWT) HIGHVO SOLAR CELL

### 2.1 Fundamentals

There are some basic features of HighVo solar cells which are common for all different types of HighVo cell concepts. The existence of several unit cells (UC) on one wafer, each with its own discrete emitter and back contact region. The electrical emitter separation between the UCs may be realized by a SiN diffusion mask or a screen printable diffusion barrier paste [7].

Narrow trenches enable a partial isolation of the UCs but still conserving the integrety of one device by remaining bridges between two neighboring UCs. In case of the MWT HighVo concept isolation trenches additionally serve as interconnection region for printing the metallization paste through them and interconnect the emitter front contact of one UC to the base contact of the neighboring UC. Filling of the trenches with the paste returns some of the original stability of the wafer. The trenches can be made by laser ablation or mechanical dicing.

### 2.2 MWT HighVo solar cell

The series interconnection in case of MWT HighVo solar cell is realized by screen printing the metallization paste of the emitter contact not only on the front of the cell but also into and through the narrow trenches. This is meant by metallization wrap through.

An MWT HighVo solar cell consists of several similar UCs defined out of one single wafer and therefore one device. Only the areas of UC1 and the last UC of a device are a little bit different due to cell layout and missing diffusion barriers. Each UC supplies about 580-600 mV at $V_{oc}$ and $V_{oc}$ of the HighVo solar cell can be varied by the total numer of UCs.

Figure 1 shows a schematic drawing of an MWT HighVo solar cell. The sketch of one UC with parts of the both neighboring UCs indicates the structure of cell arrangement and monolithic interconnection. Discrete emitter (2) and back contact regions (5) of each UC are defined on one single wafer (1), but are partially isolated by continuous trenches (4) from the front to the rear surface. The emitter contact (3) extends through the trench to the rear side base contact region of the neighboring UC. To detain the emitter from shunting two UCs through the narrow bridges a diffusion barrier (6) is required.

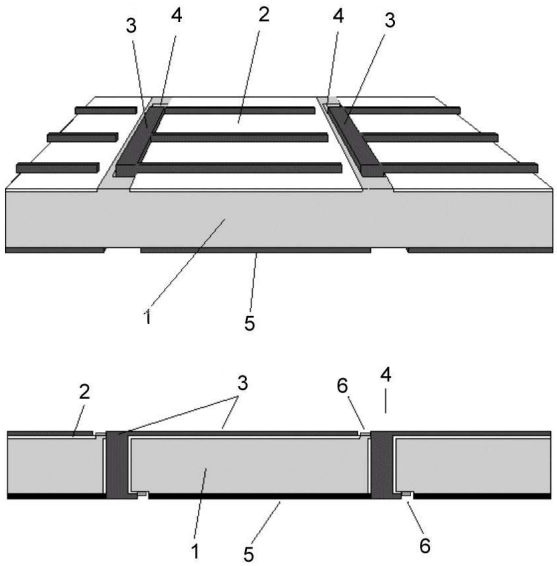


**Figure 1:** Sketch of one Unit Cell (UC) with parts of the two neighboring UCs of an MWT HighVo solar cell. 1: silicon wafer, 2: emitter, 3: emitter contact (busbar + fingers), 4: isolation trench, 5: base contact, 6: diffusion barrier.

## 3. PROCESSING

### 3.1 Process sequence

The HighVo solar cells are processed with standard processing techniques similar to industrial environment. Only the additional trench cutting step is non-standard, but if done by laser ablation it can be easily integrated in present production systems.

The base material consists of Cz silicon wafers with 330 µm thickness and a specific resistance of $\rho = 10\ \Omega$cm.

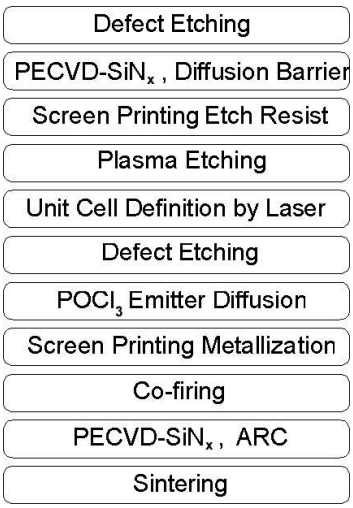


**Figure 2:** Process sequence of MWT HighVo solar cell. Trench formation is realized by laser ablation.

The process starts with a defect etching and wafer cleaning step followed by depositing 120 nm of $SiN_x$ as diffusion barrier in a Plasma Enhanced CVD reactor. To define the diffusion barrier regions by plasma etching the silicon nitride, an etch resist has to be screen printed previously. As alternative a diffusion barrier paste may be screen printed and fired [7].

During the next process step the discrete unit cells get defined by forming trenches by laser ablation. The laser damage has to be removed by alkaline etching in caustic soda, which represents a perfect possibility to integrate an implicit texture step for the mono-crystalline material resulting in randomized pyramids.

A $POCl_3$ emitter diffusion is applied resulting in different sheet resistances $R_{sheet}$ for these investigations with values between 35 Ω/sqr and 50 Ω/sqr. Emitters with higher $R_{sheet}$ than 50 or 60 Ω/sqr are currently very hard to contact with screen printed metallization.

After contacting the cells with screen printed metallization and co-firing the contacts, the process is finished by depositing a single layer $SiN_x$ anti reflection coating with PECVD. To improve the electrical properties of the metal contacts an optional sintering step may follow.

### 3.2 Experimental matrix

The objective was to investigate the influence of front surface texture and emitter sheet resistance to increase the short circuit current density $J_{sc}$ and therefore push cell efficiency. Different emitters were diffused and also MWT HighVo solar cells with random pyramid texture were investigated.

## 4. SOLAR CELL RESULTS

### 4.1 IV-Data

The geometry of the investigated MWT HighVo solar cells consists of 7 UCs and a total area of 23.8 cm², as can be seen in the photographs of figure 2. All IV-measurements were performed under standard AM1.5 illumination (100 mW/cm²) conditions at 25°C. To be able to report comparable IV-parameters with standard solar cells such as $J_{sc}$ and $V_{oc}$ we have to convert the values depending on single UC's $J_{sc,uc}$ and $V_{oc,uc}$ with respect to the total number of UCs and UC-area. The minimum UC-area of the device determines the $J_{sc}$ of the entire HighVo solar cell.

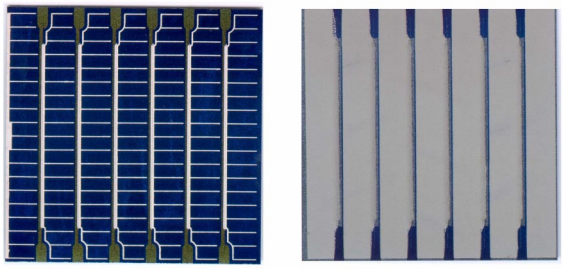

**Figure 3:** Photograph of an MWT HighVo solar cell (left: front side, right: rear side).

The average open circuit voltage per UC was calculated to $\langle V_{oc,uc} \rangle$ = 587 mV for all measured HighVo cells without texture and $\langle V_{oc,uc\ tx} \rangle$ = 591 mV for the textured cells. Normally $V_{oc}$ is expected to be lower for textured cells, but the investigated cells here were not processed in the same batch. Supposably the reason for the greater $V_{oc}$ is a more accurate processing for the textured cells. The best cell reaches $\eta$ = 12.7 % and a voltage at maximum power point

$V_{mpp}$ = 3.35 V performing a power output of P = 296 mW (figure 4).

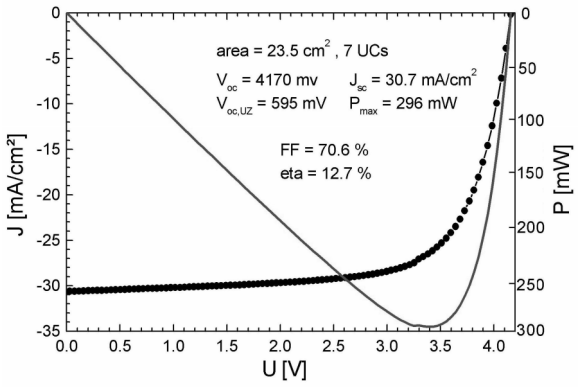


**Figure 4:** Measured IV-curve of the best textured HighVo solar cell with η = 12.7 % and $P_{max}$ = 296 mW at maximum power point.

The IV-measurements of the best cells are summarized in table I.

**Table I:** Performance parameters of the best MWT HighVo cells (7 UCs) under standard AM1.5 conditions.

| emitter [Ω/sqr] | FF [%] | η [%] | $J_{sc}$ [mA/cm²] | $V_{oc}$ [mV] | $V_{oc,UC}$ [mV] | |
|---|---|---|---|---|---|---|
| 40 | 64.8 | 10.7 | 28.7 | 4130 | 590 | |
| 35 | 68.3 | 11.3 | 28.3 | 3550 | 591 | 6 UCs |
| 35 | 70.6 | 12.7 | 30.7 | 4170 | 595 | textured |
| 50 | 56.7 | 9.4 | 29.1 | 4090 | 584 | |

The increase in $J_{sc}$ is clearly visible and the average increase in $J_{sc}$ is about 1.5 % for the use of the 50 Ω/sqr emitter compared to the 35-40 Ω/sqr emitter. The random pyramid textured surface in combination with ARC and 35 Ω/sqr emitter adds another 4-6 % increase in $J_{sc}$.

The fill factors are not satisfying yet as they do not reach values greater than 65-71 %. One reason for these low fill factors is the conceptional shunt resistance $R_{sh}$ between every two unit cells caused by the remaining bridges of p-doped bulk silicon at the edges of the device. As the base material consists of 10 Ωcm Cz silicon there exists a limitation for $R_{sh,eff}$ based on geometry design of the diffusion barrier region and the width of the bridge between trench and edge of the device. $R_{sh,eff}$ is therefore limited to about 500 Ωcm² although each UC individually reaches $R_{sh}$ of 5-10 kΩcm². A partial solution of this problem is found in the above mentioned "frame" geometry which avoids bridges of base material between neighboring UCs.

The series interconnection of mismatched UCs gives another cause for non-optimal fill factors. As the resulting IV-curve of the device is always a product of superpositionning of several mismatching single UC's IV-curves, it is obviously difficult to obtain good fill factors.

The Metallization of the trenches in combination with the back contact screen printing includes another problem producing low fill factors. If base contact Al metal paste daubs to the next UC's region across the Ag paste in the trench additional shunting occurs.

To eventually improve these weak fill factors it is necessary to both optimize the geometry of cell edges and minimize mismatches in the different UC performances.

4.2 Spectral Response Measurements

To measure the spectral response of a solar cell is a common method to specify gains in $J_{sc}$ due to the response behavior at certain wavelengths. Emitters with higher sheet resistance $R_{sheet}$ have a better blue response compared to emitters with lower $R_{sheet}$. We investigated this characteristic with our HighVo devices and the results are shown in the measurements of figure 5. The very high values of IQE in the red region can be well originated with the excellent high bulk diffusion lengths of the material.

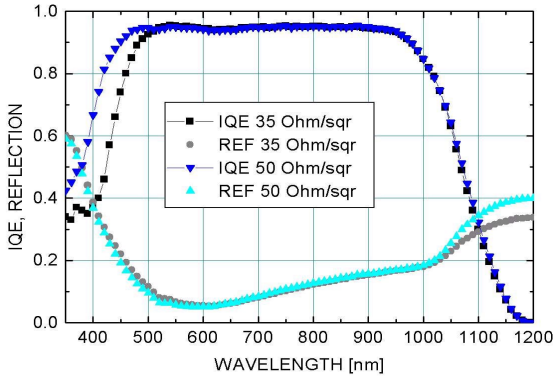


**Figure 5:** Internal Quantum Efficiencies (IQE) and reflection data of HighVos with different emitter sheet resistance $R_{sheet}$ .

Note the better blue response of the 50 Ω/sqr emitter. The vanishing differences of the reflection data are due to a common ARC process batch for the measured cells with a shared PECVD $SiN_x$ deposition.

4.3 LBIC Mappings

Besides the IV-measurements and spectral response data some of the HighVo devices were also characterized by LBIC (Light Beam Induced Current) mappings. The information in the mappings depends on the wavelength of the used laser light source and reflects the device properties in a certain depth of layer, due to the different absorption coefficients.

The mapping shown in figure 6 was made at a wavelength of λ = 980 nm and represents therefore information from the bulk and rear side of the HighVo cells.

The quadratic scaling of the plot accents varying details. The front contact in terms of finger grid and busbar of one UC is visible. It is possible to distinguish between the white base contact region with Al metallization and the non-passivated respectively non-metallized grey region. As these regions constitute of quite small areas in comparison to the overall area the decrease in $J_{sc}$ is negligible.

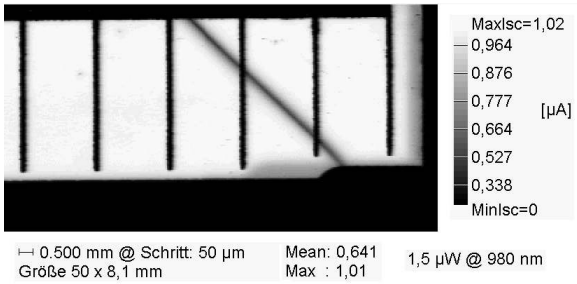


**Figure 6:** LBIC mapping of one UC at $\lambda$ = 980 nm. Back contact side is visible: white = Al contact, grey = non-passivated region and black = contact fingers and busbars of front side. The diagonal line marks a crack in the solar cell.

## 5. CONCLUSION & OUTLOOK

The concept of monolithic integrated mono-crystalline solar cells has been shown and a suitable process sequence with mostly industrial relevant process steps suggested. We have explained how to easily implement alkaline texturization and investigated the influences of different emitters and texture on $J_{sc}$. The cell results validate the possible increase in $J_{sc}$ due to emitters with higher sheet resistance and textured surface and give reason to soon reach efficiencies greater than $\eta$ = 13 % with optimized processing conditions and $J_{sc}$ matched emitters. The highest efficiency of the cells so far processed for this investigation reached up to $\eta$ = 12.7 %.

The fill factors have to be increased in future work to reach the goal of higher efficiencies and therefore we project to investigate and optimize the metallization / co-firing step on the one hand, and on the other hand we have to overcome the limitations due to moderate shunt resistances between the UCs.

## 6. ACKNOWLEDGMENTS

We like to thank M. Keil for his support in cell processing as well as B. Fischer, T. Pernau and H. Knauss for their kind suggestions with cell measurements.

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