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THE EU PROJECT R2M-SI ON ROLL TO MODULE PROCESSED CRYSTALLINE SILICON THIN-FILMS

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ABSTRACT: This paper presents a summary of the EU project "roll to module processed crystalline silicon thin-films" (R2M-Si). The aim of this project was to lift off c-Si-thin-films in a cost effective manner, and to process them to integrated interconnected solar cells. One major goal was therefore to provide Si foil material for solar cells with a high efficiency potential.
Within the R2M-Si project both the theoretical understanding and the actual process development of porosifying and detaching layers from flat wafers as well as from the circumference of a silicon rod have been investigated. Studies on crystal orientation dependence of the porosification along with tool development towards a continuous formation of a separation layer were accompanied by in depth understanding and thus optimization of the reorganization and subsequent epitaxial growth process. Finally the introduction of a special attachment process and an integrated solar cell concept could be achieved.
Keywords: c-Si Thin Film Solar Cell, Porous Silicon, Lift off

1 INTRODUCTION

The project R2M-Si which stands for "Roll to Module processed Crystalline Silicon Thin-Films" was submitted to the "ENERGY.2010.10.2-1: Future Emerging Technologies for Energy Application" call of the 7th Framework Program in 2009 and was granted to run for 3 years (2010 – 2013).
Cost reduction is still a major goal in photovoltaic development. Silicon foils offer the possibility to reduce silicon consumption and consequently allow cost reduction while maintaining the high efficiency of bulk Si solar cells.
The motivation of this project was to increase the cost-effectiveness of producing crystalline silicon thin-film lift off layers and subsequently fabricated solar cells and modules. The combination of c-Si and a thin absorber holds the potential to either tap from the wealth knowledge and expertise that is available from the bulk crystalline Si PV industry or processing sequences known from other thin film approaches. This gave our approach not only an excellent starting point for a successful development but also an inspiring fertilizing and competitive surrounding in the community.

The impact of this project lies in the conjunction of the high efficiency potential of the material and the low-cost high throughput tools necessary for this concept as well as a dedicated solar cell and module processing sequence. The joined partners in this collaboration are amongst the leading institutions working in the topic, completed by two experienced industrial companies. In accordance to the nature of the call, the R2M-Si project was set out to be a high risk endeavor with starting ground for the proposed core issues either in a very rudimentary and/or a non-existing state.

2 APPROACH AND MAIN RESEARCH TOPICS

2.1 Approach

The general approach of the R2M-Si project was to avoid bottlenecks encountered in the state of the art PV production. The main bottlenecks identified are conversion efficiency, material consumption and manufacturing complexity. The proposed solution belongs to the so-called c-Si thin-film lift-off approach, where thin crystalline silicon layers are stripped from silicon wafers.

The overall aim of the R2M-Si project was to provide a disruptive alternative to even advanced standard high-efficiency wafer and thin-film solar cells with a consumption of highly pure silicon below 0.5 g/W and a simplified module process, allowing very competitive module production cost. One special aim of this project was to enable the use of lift-off films in a nearly handling-free approach, and thereby avoid limitations by handling issues.

2.2 Main research topics

In order to accomplish those goals the critical key steps of the proposed concept were identified and elaborated in the course of the project. The identified critical key steps are listed in the following:

- Continuous separation of a thin (<10 µm) Si foil from the circumference of a monocrystalline silicon ingot, followed by:
- Attachment to a high-temperature stable substrate of large area (e.g. graphite, Sintered Silicon, or ceramics), which can also serve as module back side (Figure 1).
- High-temperature reorganization of the silicon foil followed by in-situ epitaxial thickening in an in-line chemical vapor deposition reactor, including pn-junction formation

- Processing of high-efficiency cells and formation of integrated interconnected high-voltage modules

In the subsequent chapter, the progress and the key results made in these fields are presented.

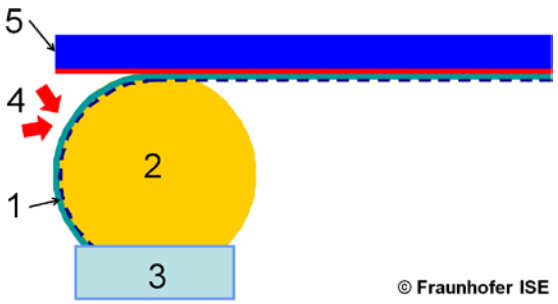

Figure 1: Schematic of the silicon layer detachment setup: A separation layer (1) is produced by immersion of a monocrystalline silicon ingot (2) in an electrochemical etch bath (3). After an optional reorganization (4) the foil can be detached and transferred to a substrate (5).

3 Progress achieved in R2M-Si

3.1 Continuous separation of a thin Si foil from the circumference of a monocrystalline silicon ingot

Within the consortium not only a deep understanding of the porosification process itself [1-5], e.g. on various crystalline orientations but also of the interaction of porosification, reorganization and epitaxial thickening [6-8] has been gathered. The etch rates for (110) oriented p^{++} Si wafers are e.g. shown in Figure 2 (top). Thereby three trends have been shown leading, after the annealing step, to smoother surface: the shortening of the anodization time, the decrease of the current density and employing electrolytes with higher HF concentration. Under these conditions, the pore structure reorganizes faster and smaller pores are obtained leading to structures closer to the equilibrium after the same annealing conditions. Triple layers can be used to have a void-free top surface, which is beneficial for epitaxial growth.
In the course of the project also a lab tool featuring some critical elements for an in-line porosification has been brought into operation. On basis of this tool the requirements for a continuous porosification machine have been identified and a corresponding patent application has been filed. Using the lab tool porous layers on both CZ and multicrystalline Si wafers and have been produced. Those were either reorganized, epitaxially thickened and then lifted or lifted right after the porosification, attached to a substrate, and then reorganized and epitaxially thickened. The tool offers the possibility to run an automatic porosification process for silicon wafers up to 156 x 156 mm². It is able to run different porosities and layer thicknesses by varying the current densities and/or the etching durations. The possibility to manufacture a stack of different layers is also provided by the tool. This allows the preparation of a high porous lift-off layer beneath a low porosity top layer. The SEM image in Figure 2 (bottom) shows the interface between such a high porosity lift-off layer on top of a monocrystalline Si carrier substrate before reorganization in the as etched state.

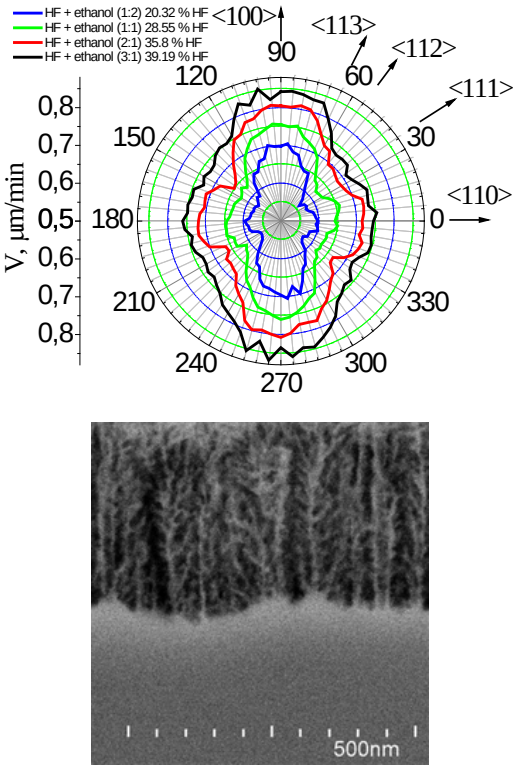

Figure 2: Top: Etch rate diagrams for (110) oriented p^{++} Si wafers. Bottom: SEM-picture of a porous to crystalline interface with the sponge like structure of the porous layer on top of a monocrystalline carrier substrate.

Within the project we were not able to set up a tool performing continuous etching on the circumference of a round crystal, due to safety restrictions which could not be resolved within the available project resources.

3.2 Attachment to a high-temperature stable substrate of large area

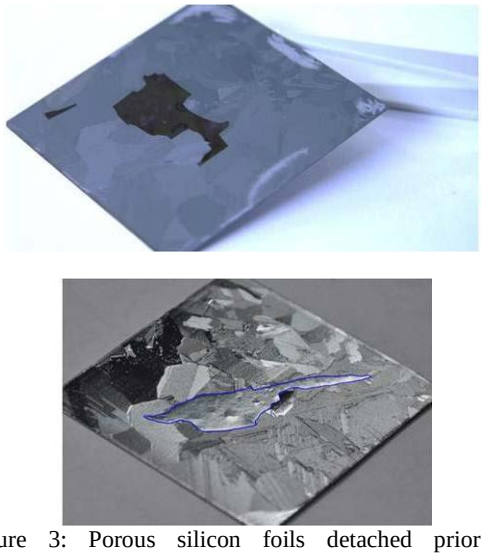

Figure 3: Porous silicon foils detached prior to reorganization and attached on mc silicon substrates (sample size 50 x 50 mm²). Top: Sample after attachment process. Bottom: Sample after reorganization and epitaxial thickening. The blue line indicates the position of the foil.

The second critical key step, attachment of the layers has also been successfully tackled. Both, epitaxially thickened and solely porous layers have been successfully transferred either to mc reference material or high-temperature stable sintered silicon substrates provided by the partner S'Tile SA. Porous silicon foils detached prior to reorganization and attached on mc silicon substrates before and after reorganization and epitaxial thickening are shown in Figure 3.

3.3 High-temperature re-organization and epitaxial thickening of the silicon foil

On reference substrates we were able to improve epitaxial quality on detachable porous silicon foils to a level exceeding requirements on a thin-film solar cell by far: lifetimes up to 150 µs at an excess hole density of 10^{16} at/cm^3 have been measured [9].

Transfer of the processes to an in-line chemical vapor deposition reactor (ConCVD) has also been successfully carried out [10]. Epitaxial layers deposited on Cz reference wafers were shiny after further process optimization based on Design of Experiments methods, as shown in Figure 4 (top). Etch pit density of these layers was 4x10^4 etch pits/cm^2 in the mean of a 6" wafer, down to 1000 pits/cm^2 locally. The latter is illustrated in Figure 4 (bottom). Effective minority carrier lifetime measurements gave values up to 3.8 µs, equivalent to approx. 70 µm of diffusion length. A further process optimization lead to in-situ deposited pn layers, where both polarities were deposited in one pass.

Application of the epitaxy process to porous silicon layers processed on 6" wafers resulted in epitaxial layers as well. Reorganization and epitaxy process still are not fully optimized, since the defect density of these layers is higher than on a bare silicon wafer surface.

3.4 Processing of thin film solar cells

In order to evaluate the best possible cell interconnection scheme for foils attached to substrates, numerical modelling was performed for an integrated interconnected module design. Full 3D simulations in Synopsys Sentaurus have been conducted to set a configuration which can be checked in a solar cell process.

Simultaneously a process to fabricate high quality epitaxial reference foils into high efficiency solar cells was also developed [11,12]. Therefore a p-type epitaxial emitter was developed along with a texturing process by TMAH etching, removing only 5 µm of the epitaxial foil and reducing the front-side reflectance to values around 12%. Other process steps like oxidation, metallization by evaporation and lithography were also adapted to the thin epitaxial foils.

By processing the foils on the front while still attached to the parent wafer, cells with efficiencies up to 14.9% were demonstrated. The cell process included a textured front side, diffused emitter and very simple Al rear-side processing. Those cells were limited by the FF (varying between 72 and 79%), most probably due to micro cracks induced during the metallization step, but also cracks due to handling during other process steps. Since it became clear that processing a free standing foil remains very difficult, but on the other hand, a rear-side reflector is essential, a porous silicon Bragg reflector was applied. Since this process can be included even before epitaxial growth, it would not make solar cell processing more complicated. The optical effects of the Bragg reflector result in a slight increase in current density; but more important is probably the appositive effect of the Bragg reflector to lower the stress in the epitaxial stack. Efficiencies up to 15.2% were obtained.

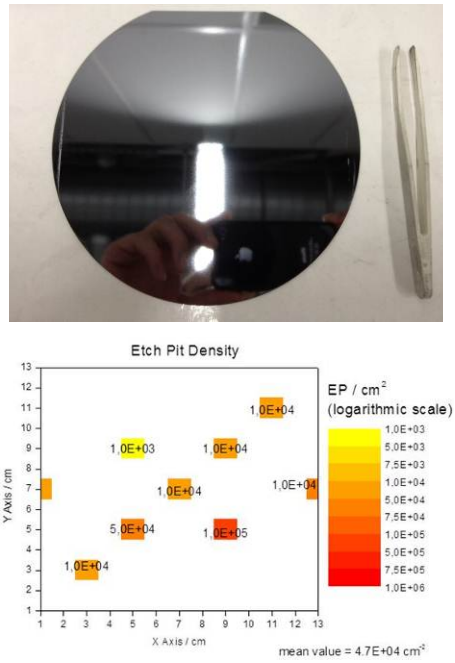

Figure 4: Top: Photograph of a 6" Cz wafer epitaxially thickened in the optimized setup of the ConCVD. Bottom: EPD map of a 6" Cz substrate after epitaxial thickening.

3.5 Integrated interconnection development

A laboratory process for integrated interconnected crystalline thin film cells was also realized [13, 14]. A sketch of the structure is shown in Figure 5 (top), and a picture of the realized structure (bottom). The active layer consisting of a 5 µm BSF layer with a doping concentration of $1 \cdot 10^{18}$ cm^{-3} and a base of 30 µm with a doping concentration of $4 \cdot 10^{16}$ cm^{-3} was grown in a lab-type APCVD (Atmospheric Pressure Chemical Vapor Deposition) reactor on silicon on insulator oxide (SOI) wafers. The best module exhibits an efficiency of 8.8 %, including the trenches between the cells and excluding the contacting pads for the measurements. V_{oc} and J_{sc} values are as expected for this architecture in the range of 600 mV and 27 mA/cm² (30 µm base with non-textured front surface). For this 5 cell module an open circuit voltage of over 3 V has been shown. The most significant shortcoming in these cells lies in the Fill Factor which turned out to be largely influenced by the series resistance. The high series resistance originated mainly from contacting problems like peeled off contacts and missing interconnection, as well as a low rear side conductivity. Solutions for improved contacting, adjustments of the doping profile, and integration of texturing are proposed. Simulations showed that an efficiency of around 18.6% is reachable providing that rear side conductivity is increased by adjusting the BSF thickness rather than its doping. With these measures a highly efficient mini-module should well be possible.

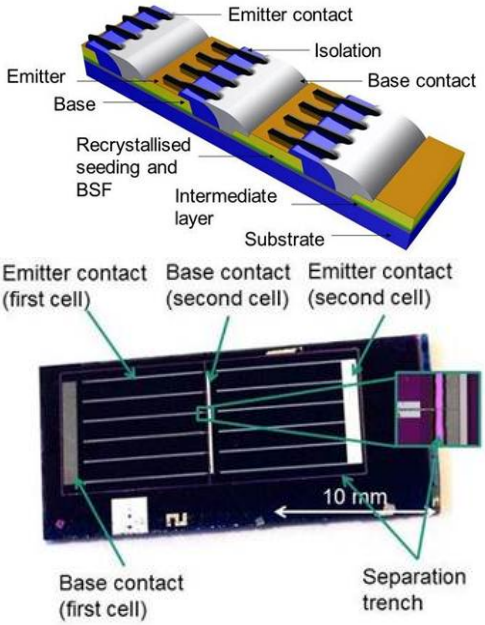

Figure 5: Top: Detail of integrated interconnected module with screen-printing interconnection (not to scale). Bottom: Mini-module consisting of two cells with 10 mm cell width each.

4 SUMMARY

Several start-ups as well as an increasing number of publications in the scientific PV community dealing with comparable approaches show the generally growing interest in the c-Si-thin-film topic. However all of them have to target similar topics: conversion efficiency, material consumption and manufacturing complexity. The topics were addressed in the EU-FET project R2M-Si by a combination of c-Si and a thin lifted absorber which sketched a path towards overcoming these obstacles, by introducing a new c-Si thin-film lift-off approach implying the potential for highly efficient solar cells at reduced costs. Key technologies like porosification, in-line-reorganization and in-line-epitaxy along with a tailored integrated cell/module concept have been addressed thoroughly and solutions have been presented.

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